



HN01.001  
HN01.002  
3

| SYSTEM | C/D     |
|--------|---------|
| PR 22  |         |
| IN P   | OUT P/S |



# PCH Strapping

| Name                  | Schematics Notes                                                                                                                                                                                                                                                                  |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPKR                  | <b>Reboot option at power-up</b><br><b>Default Mode:</b> Internal weak Pull-down.<br><b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.                                                                                        |
| INIT3_3V#             | Weak internal pull-down. Do not pull high.                                                                                                                                                                                                                                        |
| GNT3#/GPIO55          | <b>Default Mode:</b> Internal pull-up.<br><b>Low (0) = Top Block Swap Mode</b> (Connect to ground with 4.7-kΩ weak pull-down resistor).                                                                                                                                           |
| INTVRMEN              | <b>High (1) = Integrated VRM is enabled</b><br><b>Low (0) = Integrated VRM is disabled</b>                                                                                                                                                                                        |
| GNT0#, GNT1#          | <b>Default (SPI):</b> Left both GNT0# and GNT1# floating. No pull up required.<br><b>Boot from PCI:</b> Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.<br><b>Boot from LPC:</b> Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. |
| GNT2#/GPIO53          | <b>Default - Internal pull-up.</b><br><b>Low (0)=</b> Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).                                                                                                                                    |
| GPI033                | <b>Default:</b> Do not pull low.<br><b>Disable ME in Manufacturing Mode:</b> Connect to ground with 1-kΩ pull-down resistor.                                                                                                                                                      |
| SPI_MOSI              | <b>Enable iTPM:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor<br><b>Disable iTPM:</b> Left floating, no pull-down required.                                                                                                                                             |
| NV_ALE                | <b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.<br><b>Disable Danbury:</b> Connect to ground with 4.7-kΩ weak pull-down resistor.                                                                                                                     |
| NC_CLE                | Weak internal pull-up. Do not pull low.                                                                                                                                                                                                                                           |
| HAD_DOCK_EN#/GPIO[33] | <b>Low (0):</b> Flash Descriptor Security will be overridden.<br><b>High (1) :</b> Flash Descriptor Security will be in effect.                                                                                                                                                   |
| HDA_SDO               | Weak internal pull-down. Do not pull high.                                                                                                                                                                                                                                        |
| HDA_SYNC              | Weak internal pull-down. Do not pull high.                                                                                                                                                                                                                                        |
| GPI015                | Weak internal pull-down. Do not pull high.                                                                                                                                                                                                                                        |
| GPI08                 | Weak internal pull-up. Do not pull low.                                                                                                                                                                                                                                           |
| GPI027                | <b>Default = Do not connect (floating)</b><br>High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.<br>Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.                     |

# Processor Strapping

| Pin Name | Strap Description                                                 | Configuration (Default value for each bit is 1 unless specified otherwise)                                                                                                                                                                                                                                                                                      | Default Value |
|----------|-------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| CFG[4]   | <b>Embedded DisplayPort Presence</b>                              | 1: Disabled - No Physical Display Port attached to Embedded DisplayPort.<br>0: Enabled - An external Display Port device is connected to the Embedded Display Port.                                                                                                                                                                                             | 1             |
| CFG[3]   | <b>PCI-Express Static Lane Reversal</b>                           | 1: Normal Operation.<br>0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...                                                                                                                                                                                                                                                                                          | 1             |
| CFG[0]   | <b>PCI-Express Configuration Select</b>                           | 1: Single PCI-Express Graphics<br>0: Bifurcation enabled                                                                                                                                                                                                                                                                                                        | 1             |
| CFG[7]   | <b>Reserved - Temporarily used for early Clarksfield samples.</b> | <b>Clarksfield (only for early samples pre-ES1) -</b> Connect to GND with 3.01K Ohm/5% resistor<br><b>Note:</b> Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].<br>For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality. | 0             |

## USB Table

## PCIE Routing

|       |           |
|-------|-----------|
| LANE1 | LAN       |
| LANE2 | MiniCard1 |
| LANE3 | MiniCard2 |

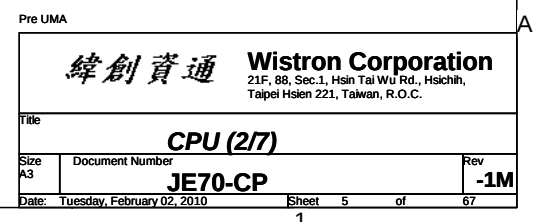
| Pair | Device       |
|------|--------------|
| 0    | USB3         |
| 1    | USB2         |
| 2    | USB4         |
| 3    | MINICARD1    |
| 4    | WECAM        |
| 5    | Touch Panel  |
| 6    | NC           |
| 7    | NC           |
| 8    | NC           |
| 9    | USB1(HS)     |
| 10   | Finger Print |
| 11   | Blue Tooth   |
| 12   | MINIC2       |
| 13   | Cardreader   |

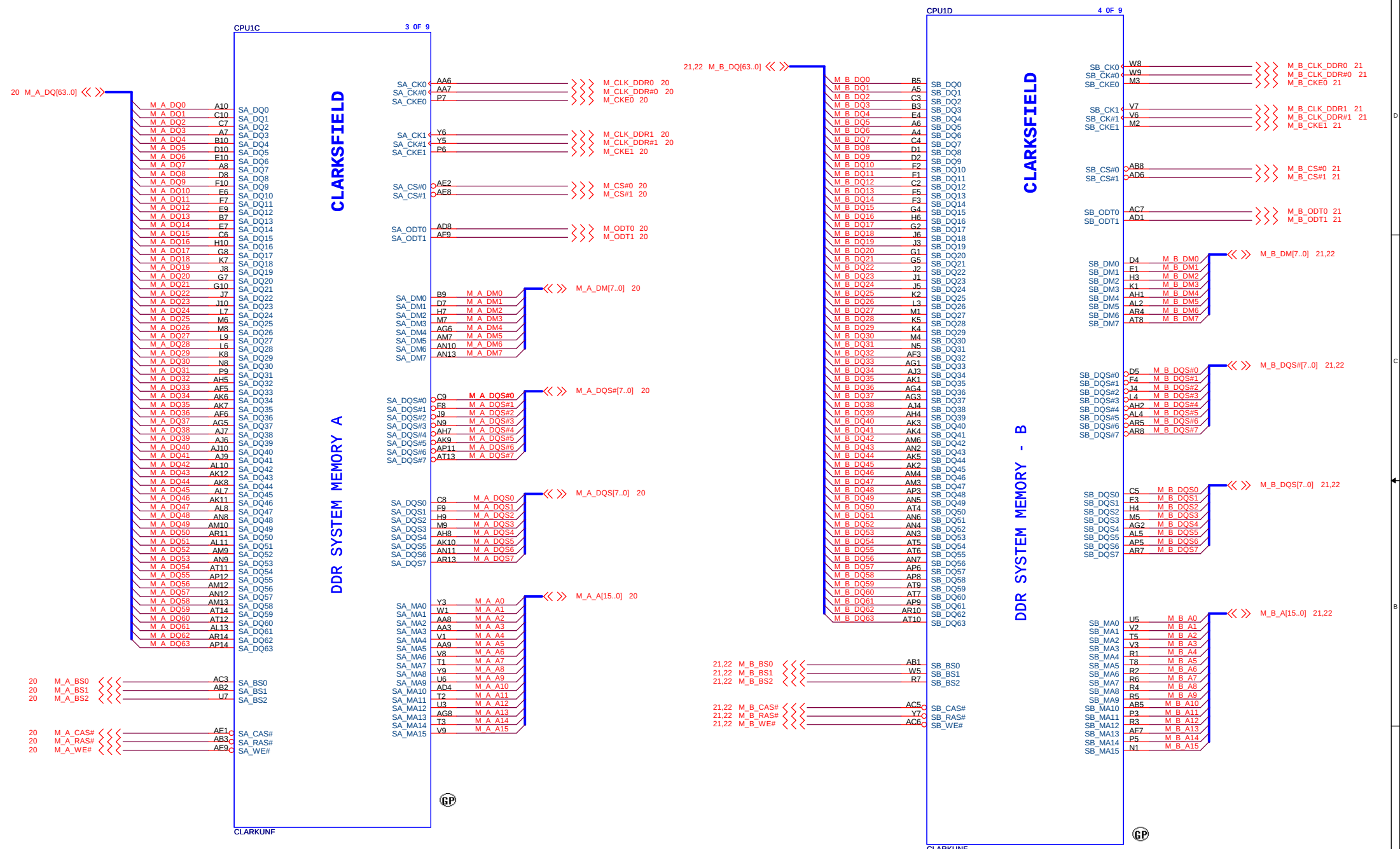
Pre UMA

|                                  |                                   |                                                                                                             |                   |
|----------------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------|-------------------|
| <b>緯創資通</b>                      |                                   | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                   |
| Title                            |                                   |                                                                                                             |                   |
| <b>Table of Content</b>          |                                   |                                                                                                             |                   |
| Size<br>A3                       | Document Number<br><b>JE70-CP</b> |                                                                                                             | Rev<br><b>-1M</b> |
| Date: Tuesday, February 02, 2010 | Sheet 2                           | of                                                                                                          | 67                |









62.10053.561

2ND = 62.10055.321

62.10053.561

2ND = 62.10055.321

Pre UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (3/7)

Size

A3

Document Number

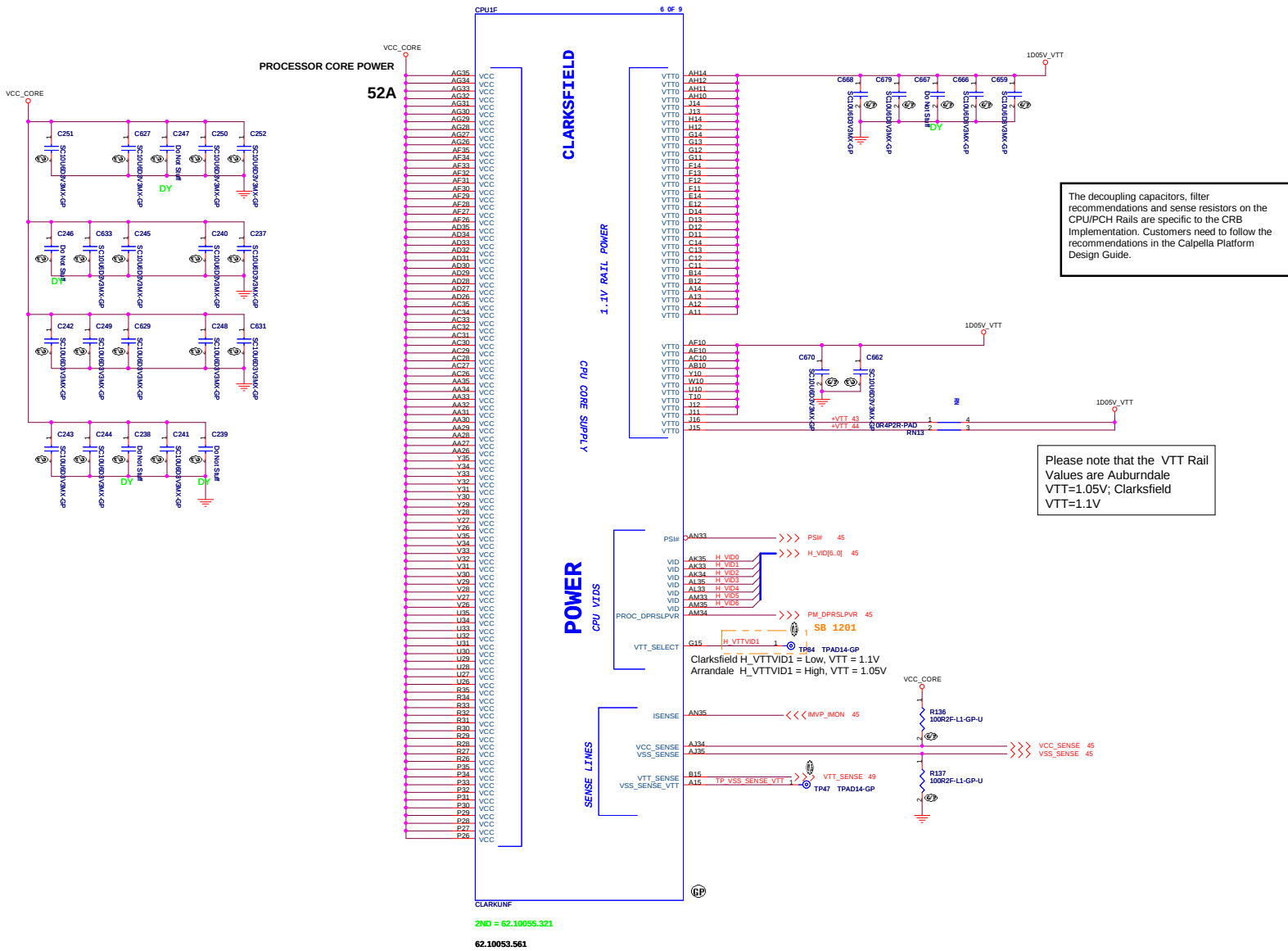
JE70-CP

Rev

-1M

Date: Tuesday, February 02, 2010

Sheet 6 of 67

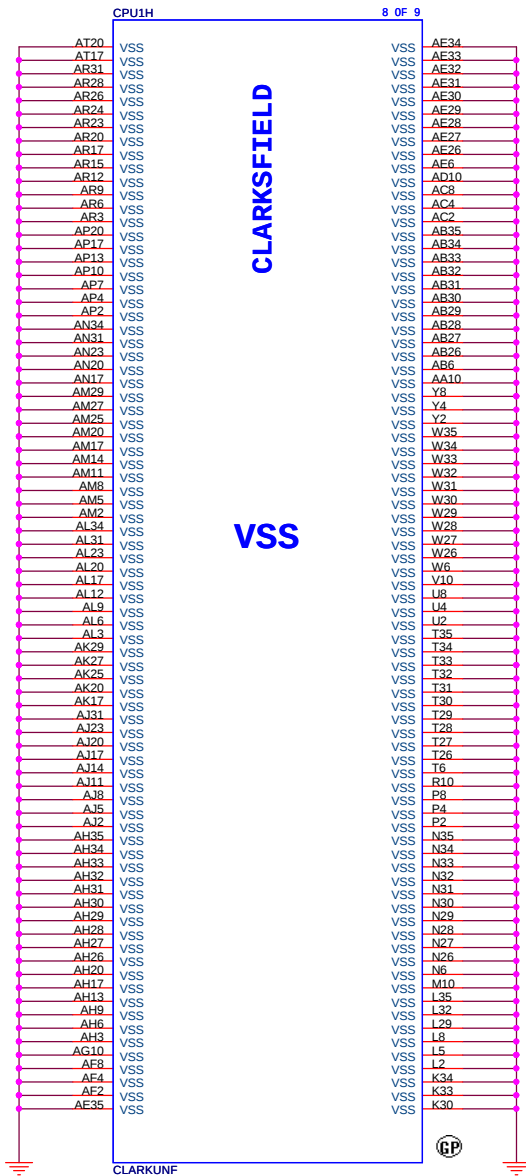


The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarkfield VTT=1.1V

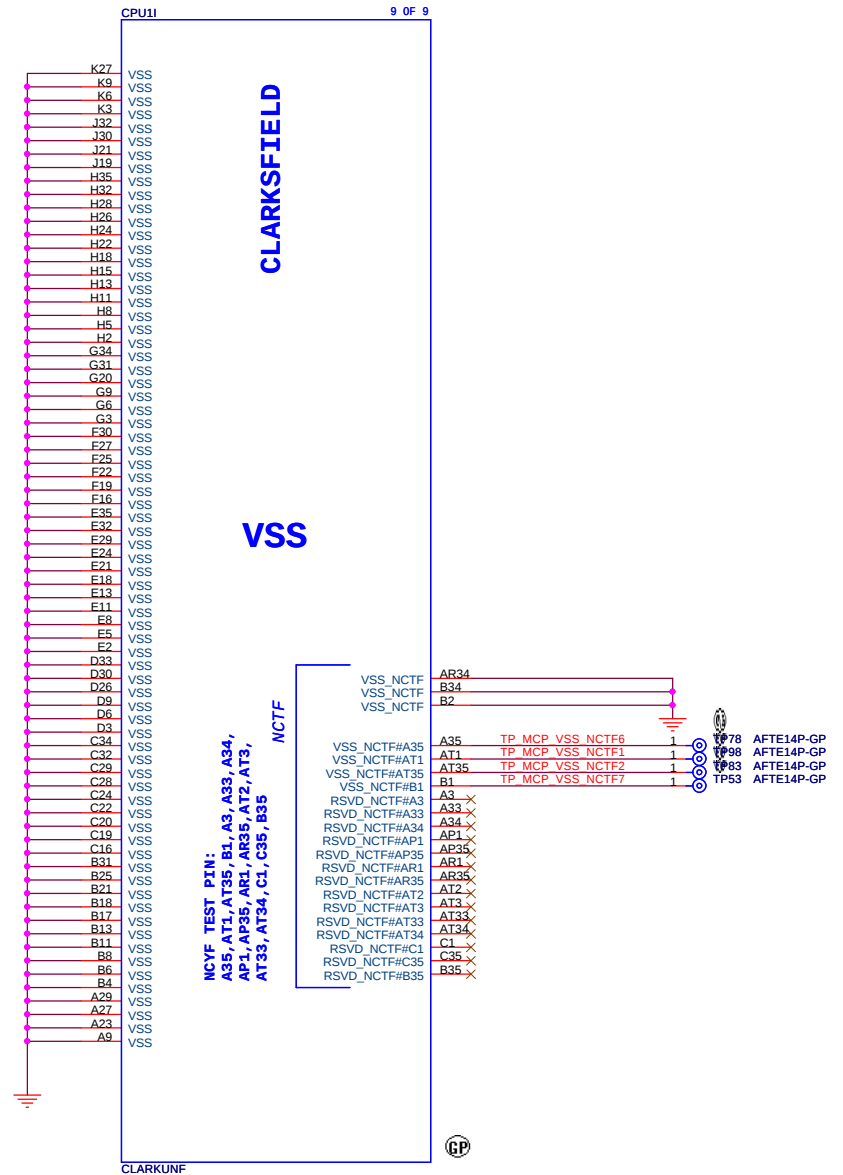
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62.10053.561





2ND = 62.10055.321

62.10053.561



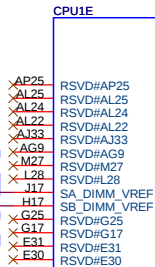
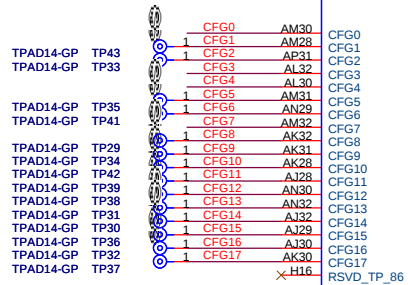
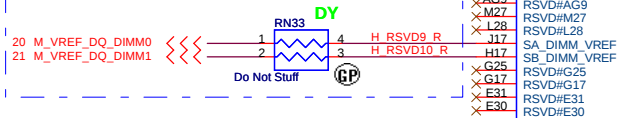
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Pre UMA

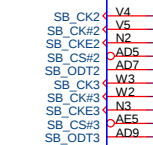
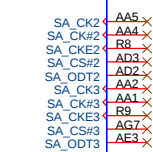
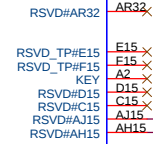
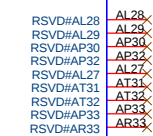
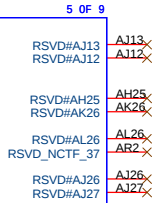
|                                                                                                                  |                 |     |
|------------------------------------------------------------------------------------------------------------------|-----------------|-----|
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| Title                                                                                                            |                 |     |
| CPU (6/7)                                                                                                        |                 |     |
| Size                                                                                                             | Document Number | Rev |
| A3                                                                                                               | JE70-CP         | -1M |
| Date: Tuesday, February 02, 2010                                                                                 | Sheet 9 of 67   |     |

## SO-DIMM VREFDQ (M3) Circuit for Clarkfield Processor

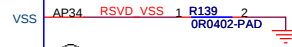
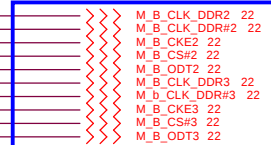


CLARKFIELD

RESERVED



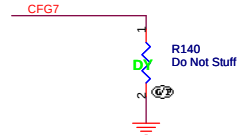
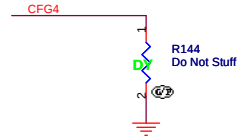
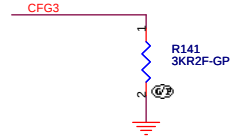
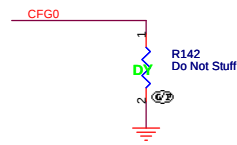
SA 1013



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

2ND = 62.10055.321

62.10053.561



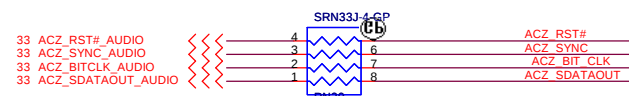
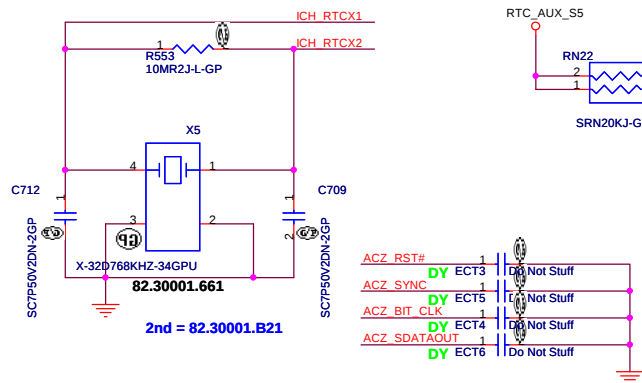
| PCI-Express Configuration Select |                                       |
|----------------------------------|---------------------------------------|
| CFG0                             | 1:Single PEG<br>0:Bifurcation enabled |

| CFG3 - PCI-Express Static Lane Reversal |                                                                          |
|-----------------------------------------|--------------------------------------------------------------------------|
| CFG3                                    | 1 :Normal Operation<br>0 :Lane Numbers Reversed<br>15 -> 0, 14 -> 1, ... |

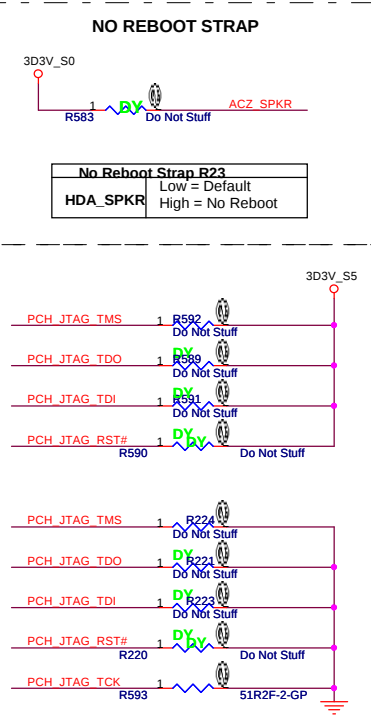
| CFG4 - Display Port Presence |                                                                                                                                                                |
|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFG4                         | 1:Disabled; No Physical Display Port attached to Embedded Display Port<br>0:Enabled; An external Display Port device is connected to the Embedded Display Port |

| CFG7(Reserved) - Temporarily used for early Clarkfield samples. |                                                                                                                                                                                                                                                                                                                                           |
|-----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFG7                                                            | Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.<br><br>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality. |

Pre UMA

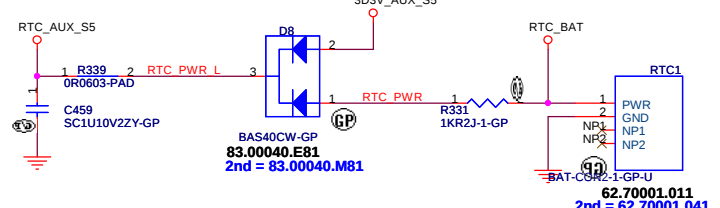
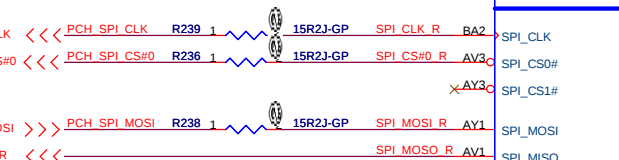


1D5V\_S0 1 R549 ACZ\_SYNC  
Do Not Stuff  
This signal has a weak internal pull down.  
On Die PLL VR is supplied by 1.5V when  
sampled high, 1.8 V when sampled low.



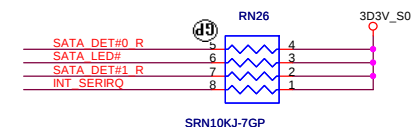
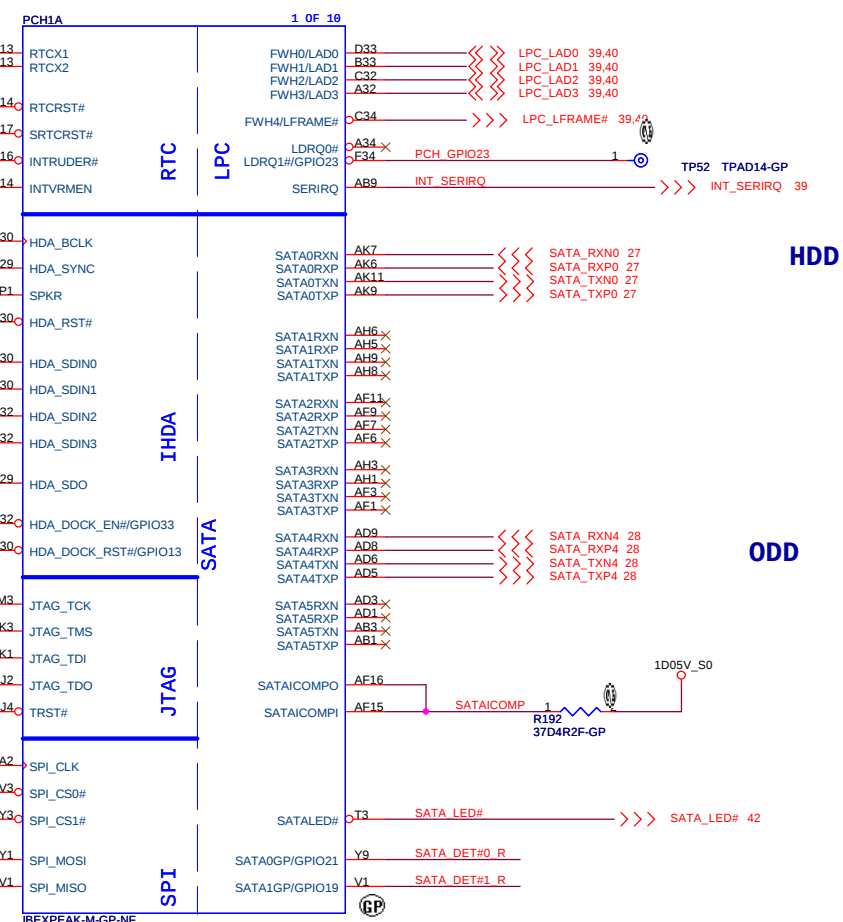
SPI\_CS0#, SPI\_MISO, SPI\_MOSI, SPI\_CLK:  
No series resistor required if routing length is 1.5"-6.5"

**SPI\_MOSI** Enable iTPM: Connect to Vcc3\_3 with  
8.2-kΩ weak pull-up resistor.  
Disable iTPM: Left floating, no  
pull-down required

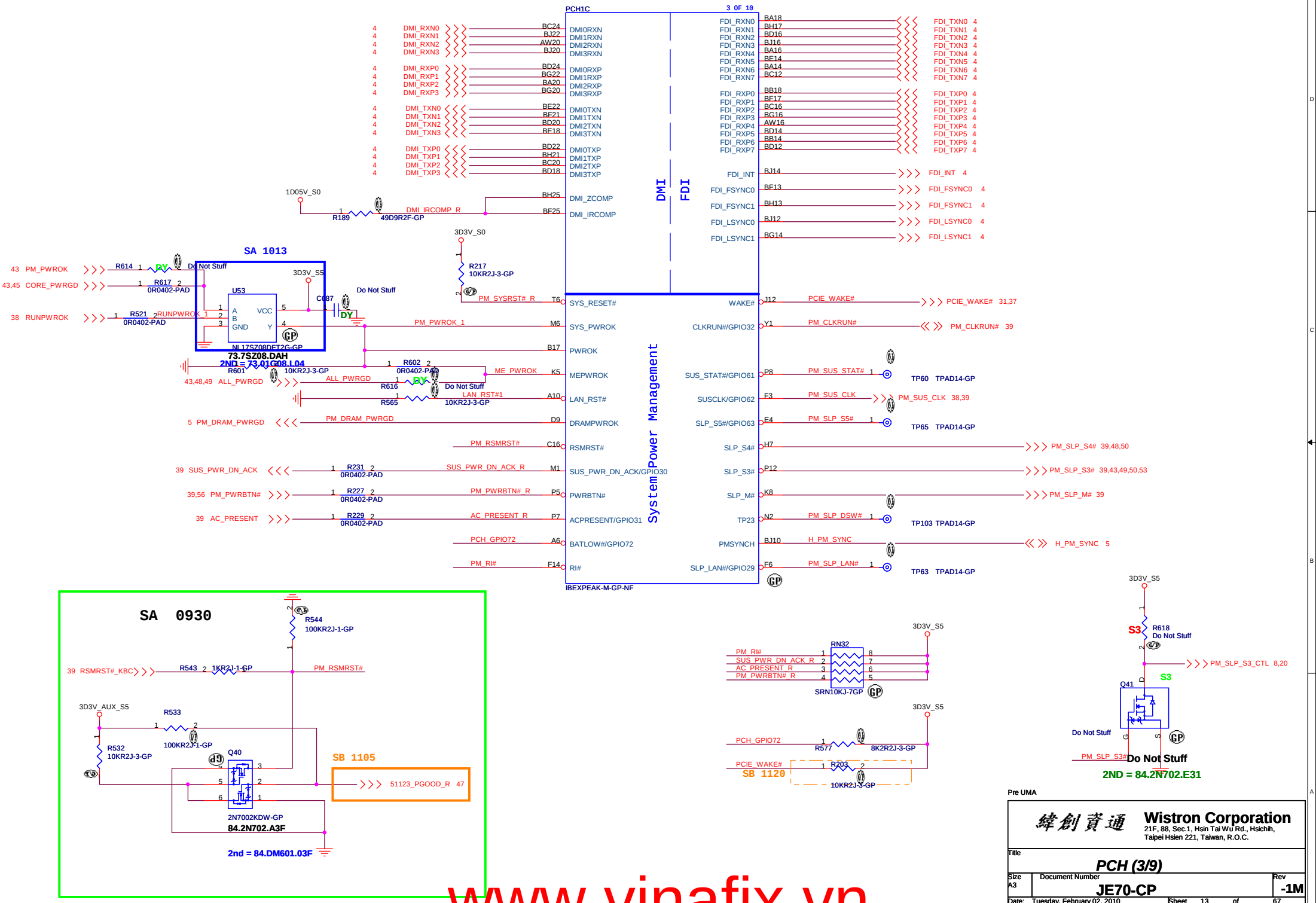


INTVRMEN- Integrated SUS  
1.1V VRM Enable  
High - Enable internal VRs

|                                          |             |             |
|------------------------------------------|-------------|-------------|
| Integrated VccSus1_05,VccSus1_5,VccCL1_5 |             |             |
| INTVRMEN                                 | High=Enable | Low=Disable |
| Integrated VccLan1_05VccCL1_05           |             |             |
| LAN100_SLP                               | High=Enable | Low=Disable |







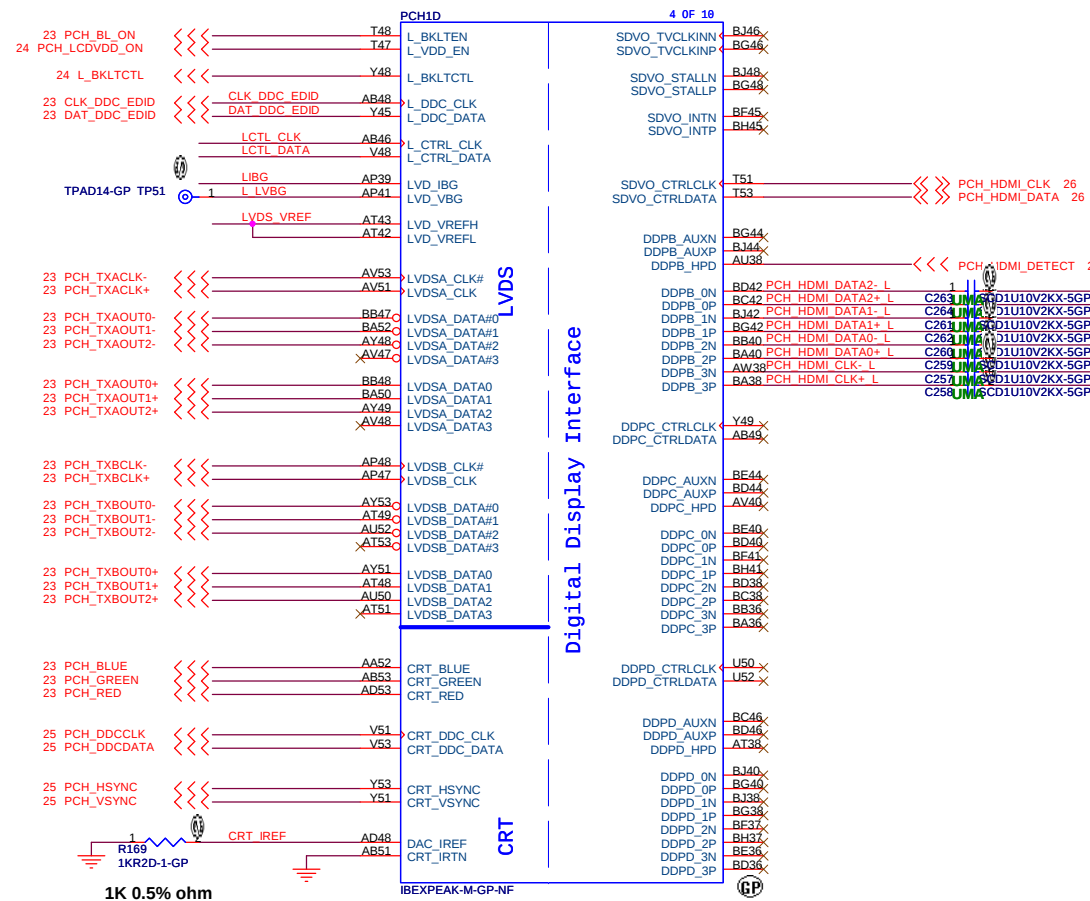
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UMA\_PX

UMA\_PX

UMA PX

UMA\_PX

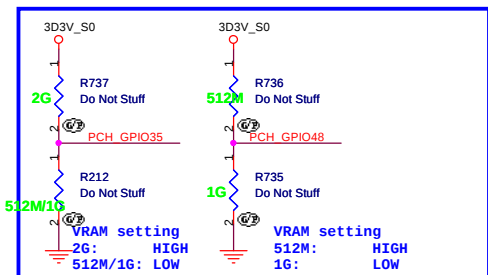
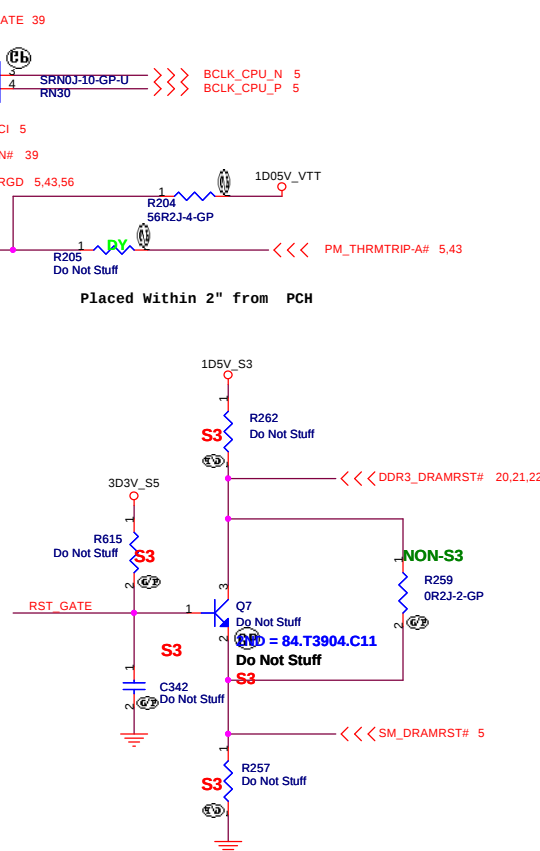
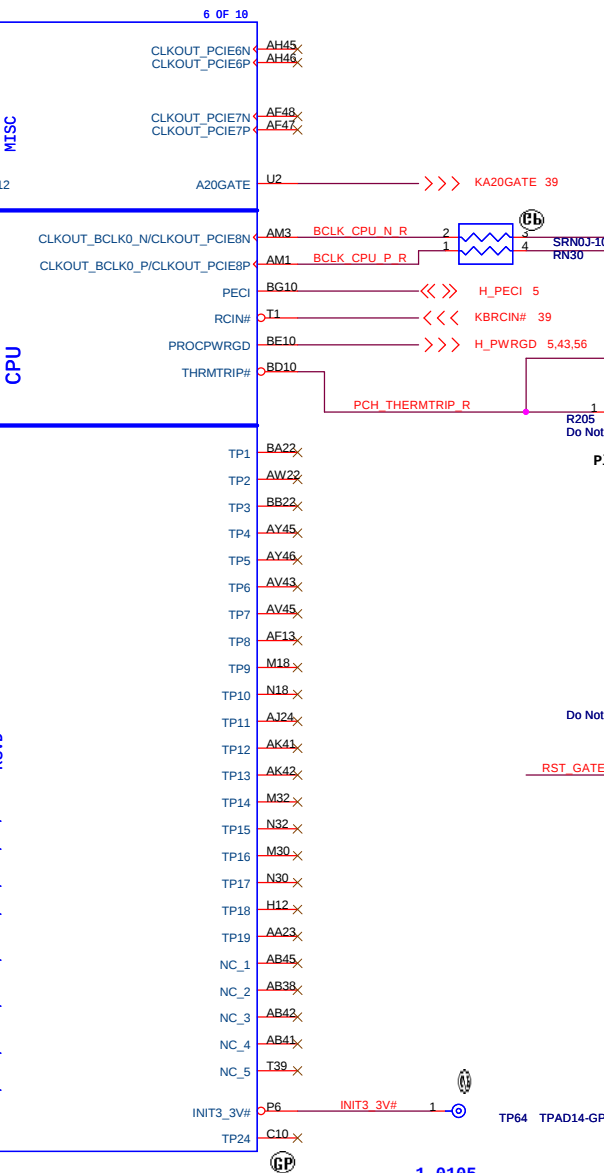
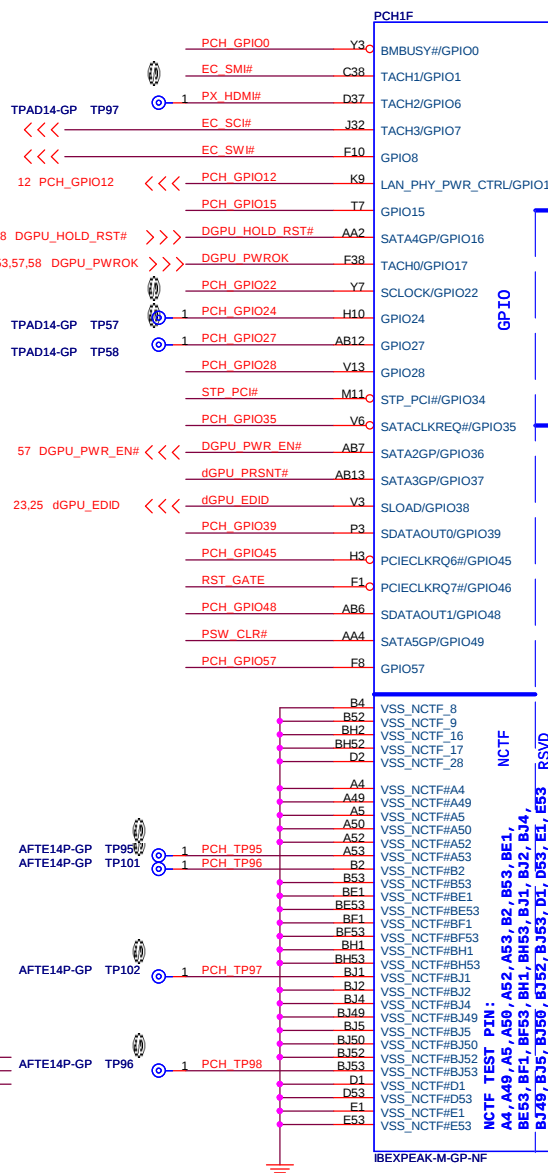
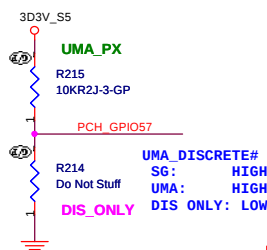
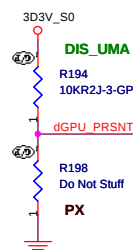
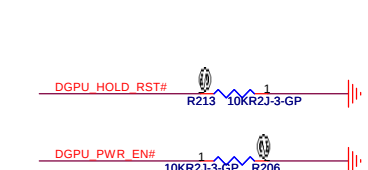
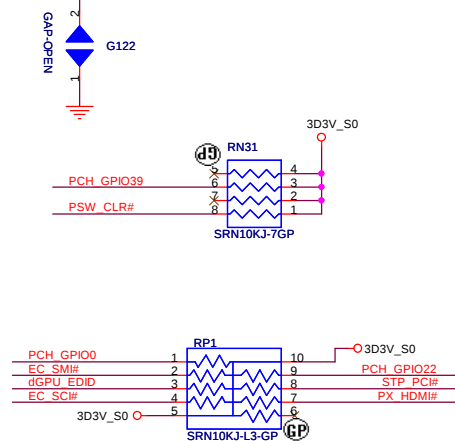


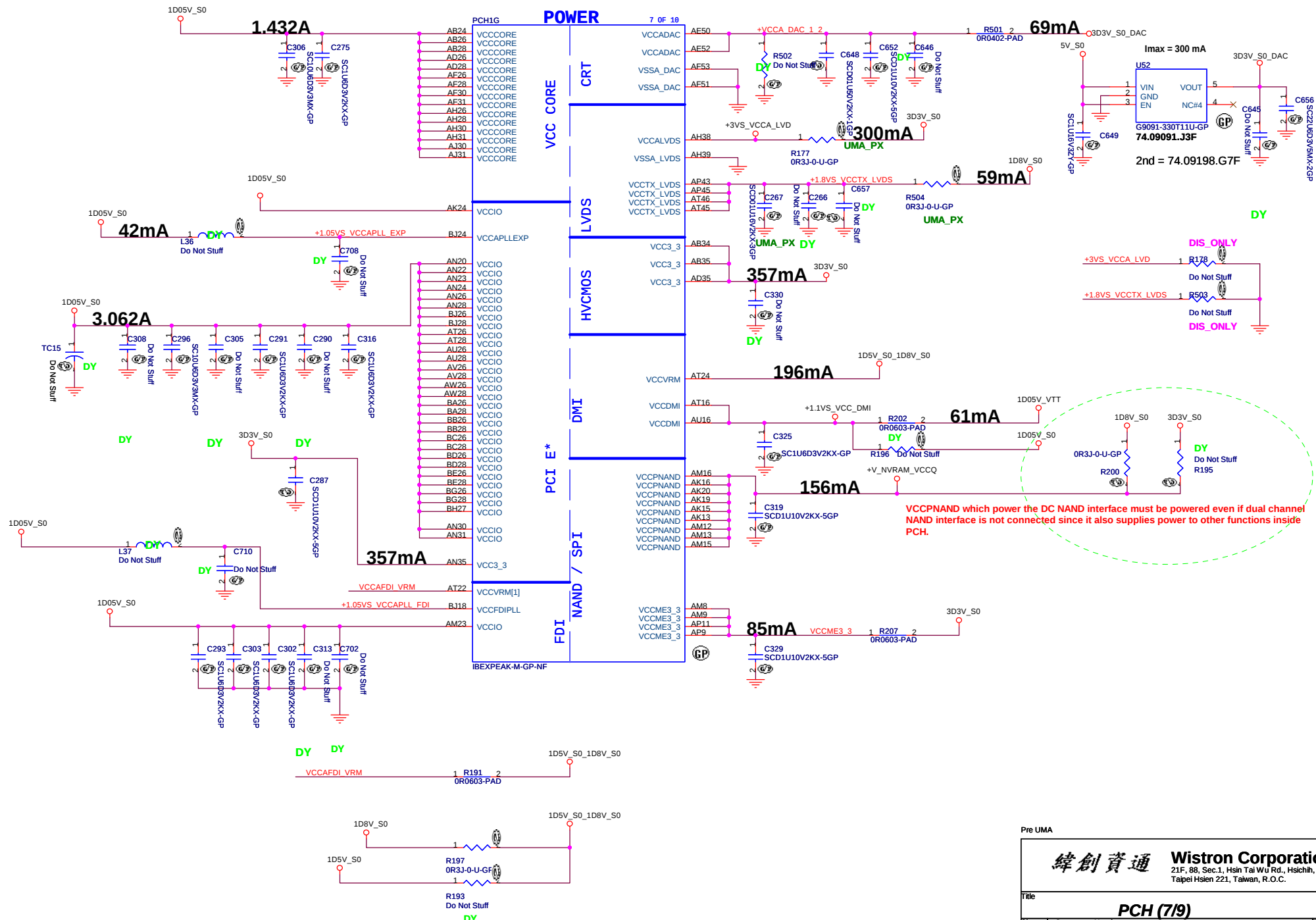
Pre UMA

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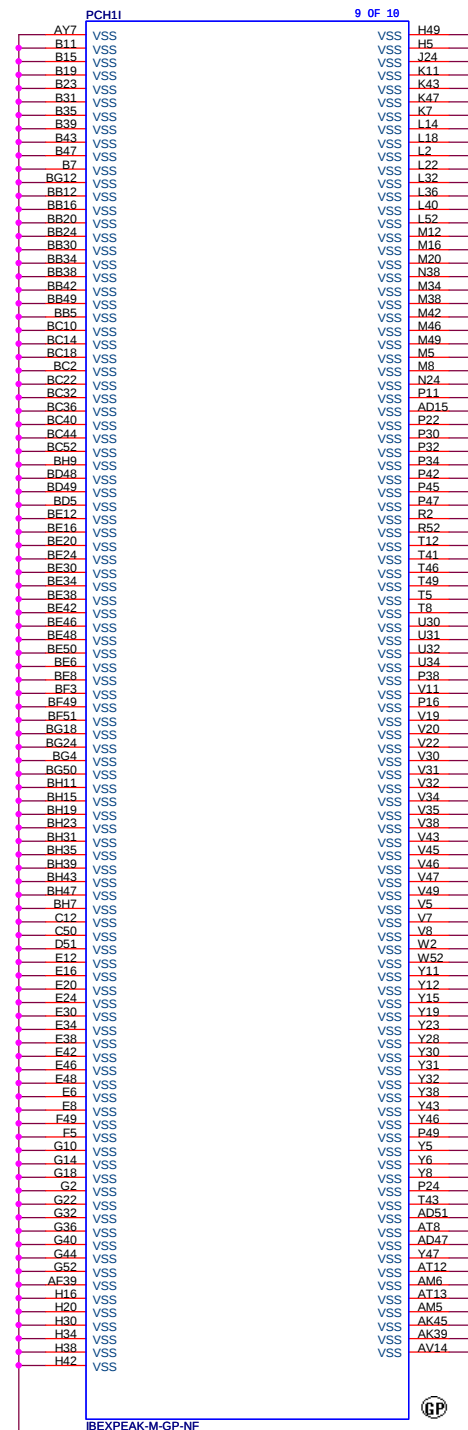
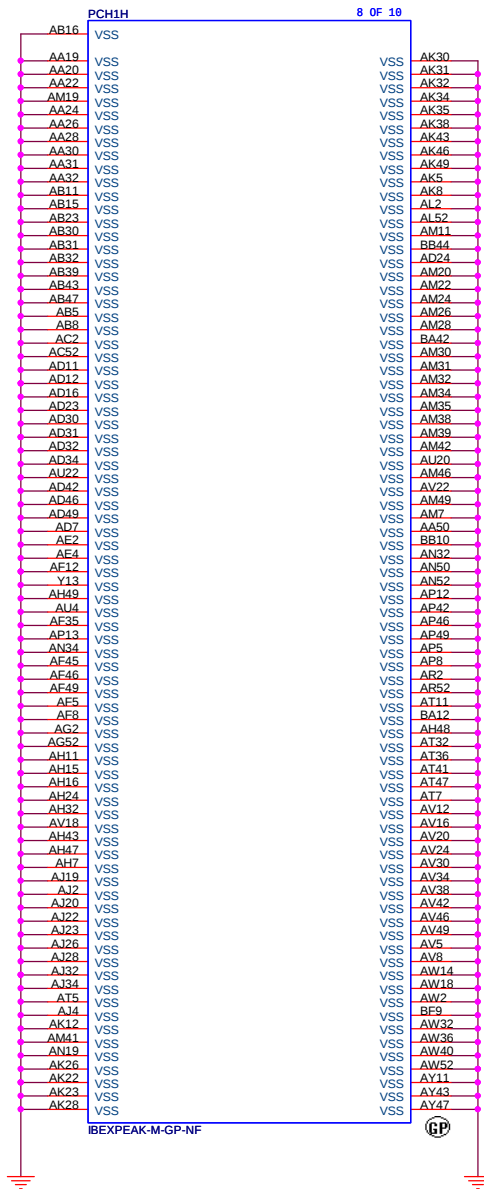


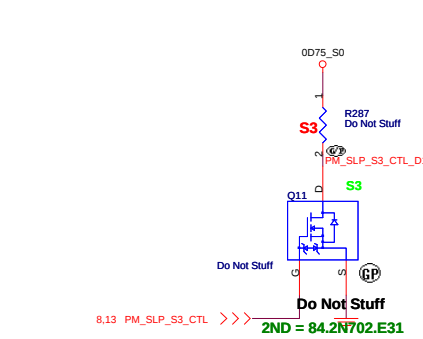
GPIO15 has a weak[20K] internal pull down.  
No need to have external pull up/down.  
GPIO 15 pin is set to low at reset.  
Low : ME Crypto TLS with no confidentiality  
High : ME Crypto TLS with confidentiality



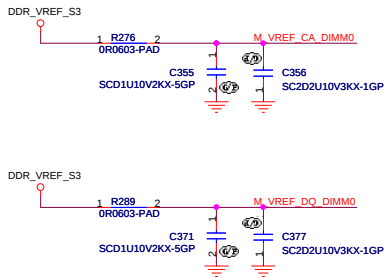




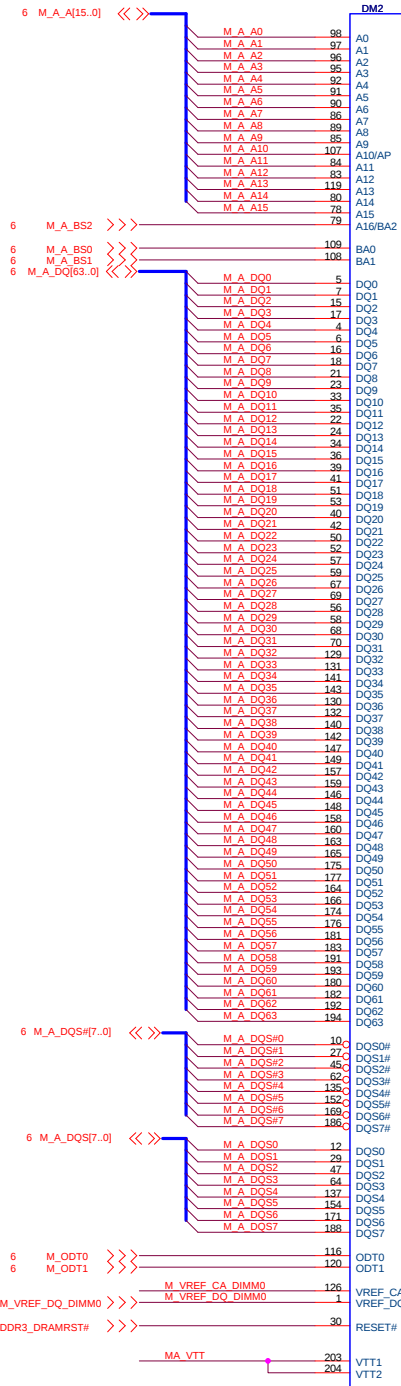
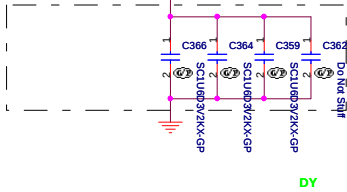




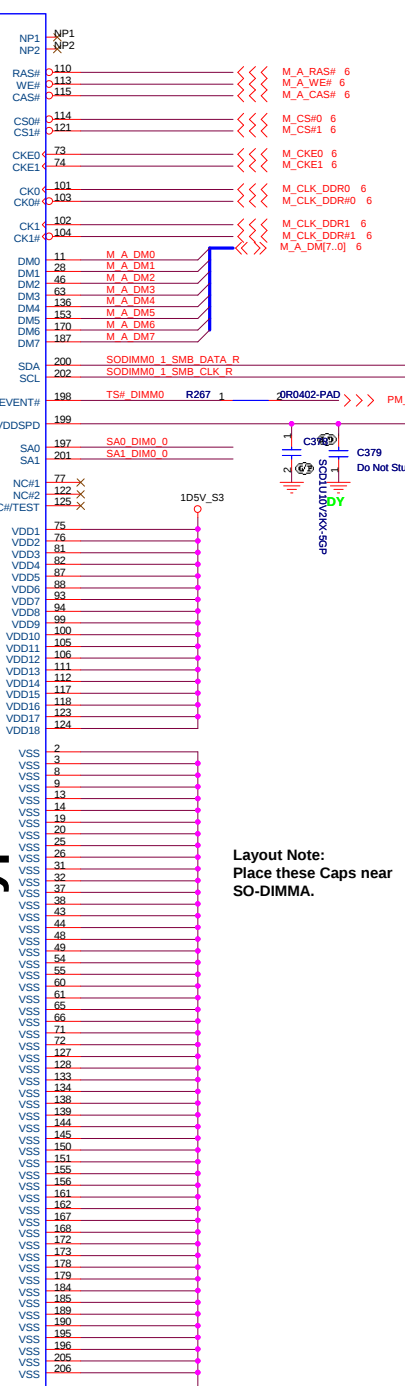
8.13 PM\_SLP\_S3\_CTL >>> 2ND = 84.2N702.E31



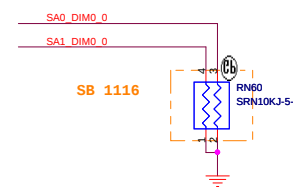
Place these caps close to VTT1 and VTT2.



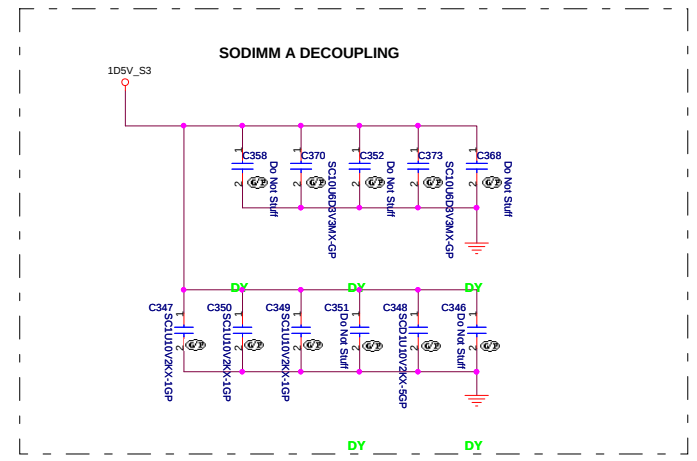
Standard type



Layout Note:  
Place these Caps near SO-DIMMA.



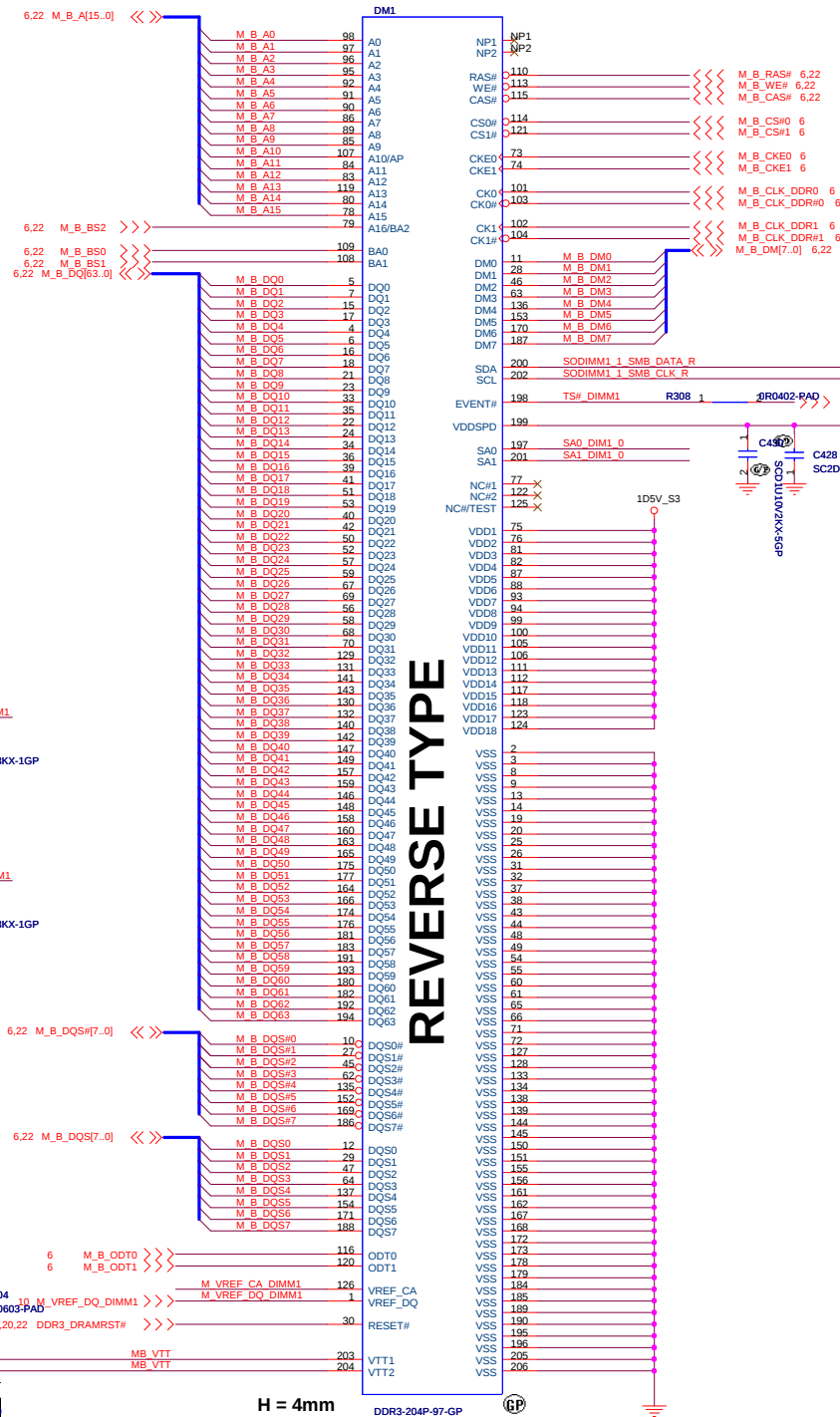
Note:  
If SA0\_DIMM0 = 0, SA1\_DIMM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30  
  
If SA0\_DIMM0 = 1, SA1\_DIMM0 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32



Pre UMA

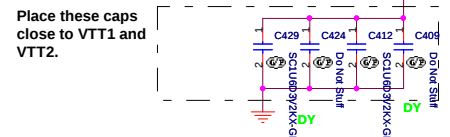
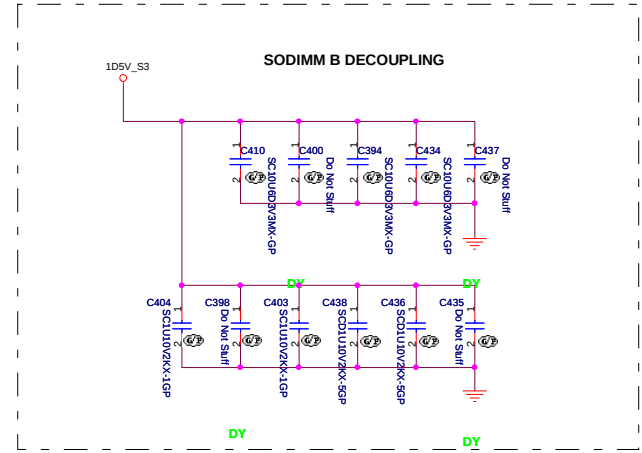
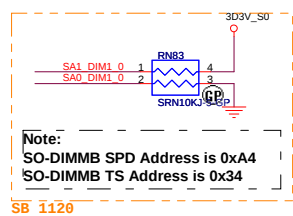
|                                                                                                                     |                                 |
|---------------------------------------------------------------------------------------------------------------------|---------------------------------|
| <b>緯創資通</b><br>Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                                 |
| Title: <b>DDR3 Socket DM1</b>                                                                                       |                                 |
| Size: Custom                                                                                                        | Document Number: <b>JE70-CP</b> |
| Date: Tuesday, February 02, 2010                                                                                    | Sheet 20 of 67                  |

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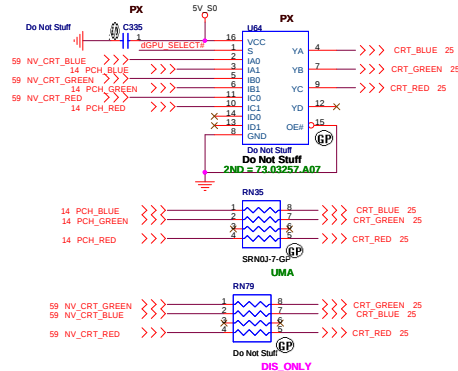
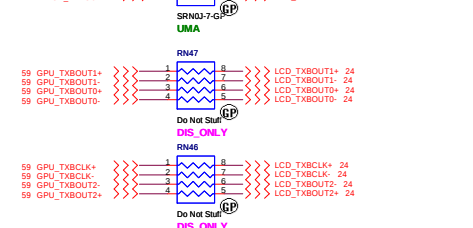
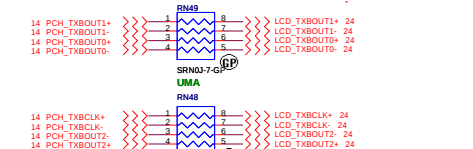
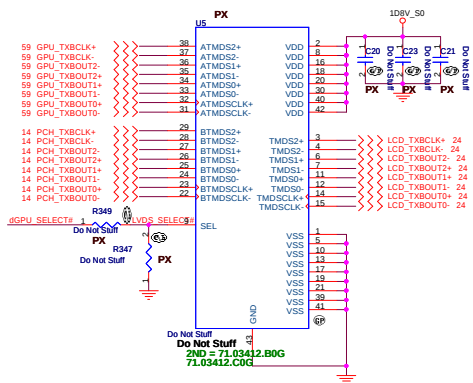
REVERSE TYPE

H = 4mm  
DDR3-204P-9T-GP  
62.10017.W11  
2ND = 62.10017.V51

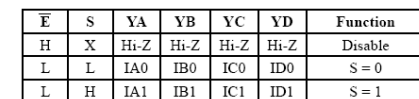


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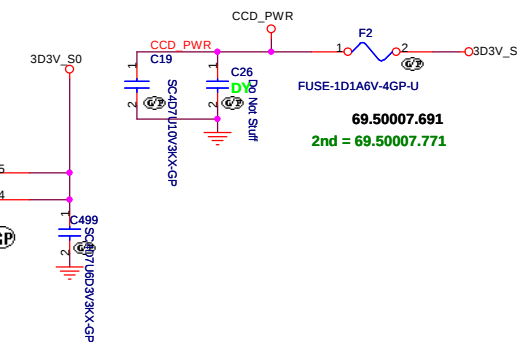
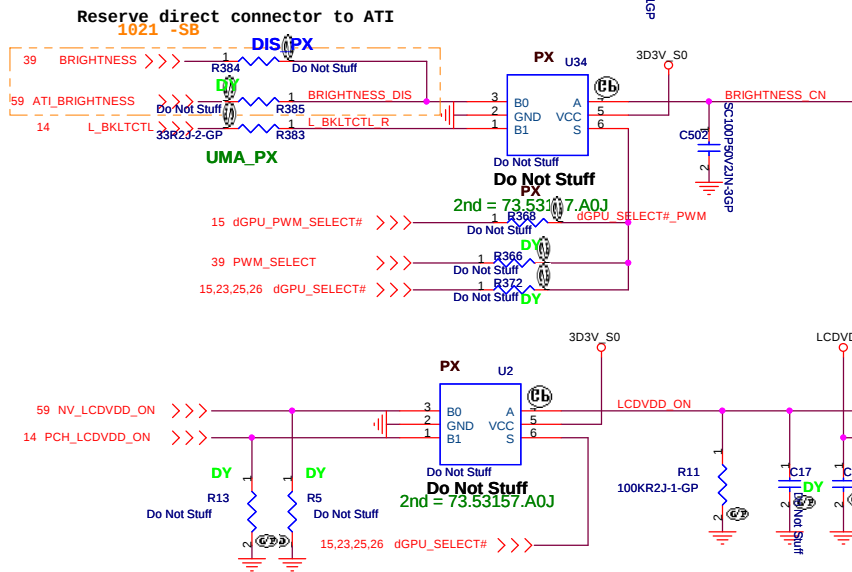
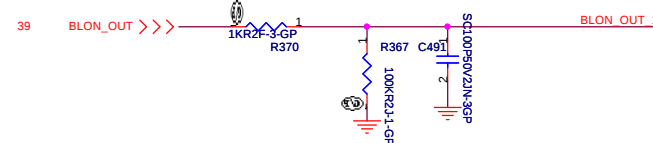
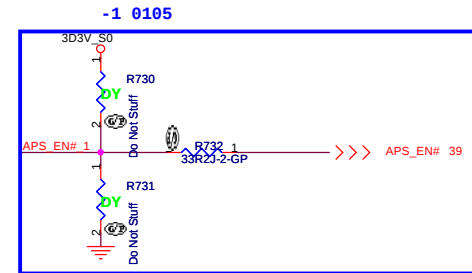
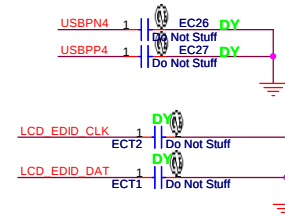
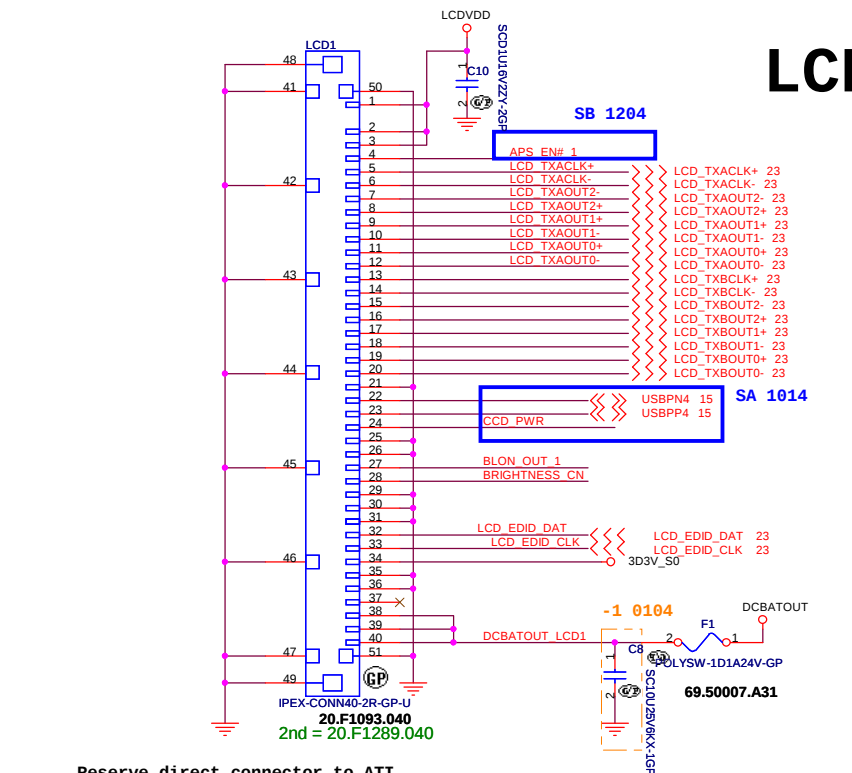




| FUNCTION TABLE |                            |          |
|----------------|----------------------------|----------|
| SEL            | FUNCTION                   | OUTPUT   |
| L              | TMDSn+ = ATMDSn+           |          |
|                | TMDSn- = ATMDSn-           |          |
|                | TMDSCLK+ = ATMDSCLK+       | TMDSn+   |
|                | TMDSCLK- = ATMDSCLK-       | TMDSn-   |
|                | BTMDSn+ = High Impedance   | TMDSCLK+ |
|                | BTMDSn- = High Impedance   | TMDSCLK- |
| H              | BTMDSCLK+ = High Impedance |          |
|                | BTMDSCLK- = High Impedance |          |
|                | TMDSn+ = BTMDSn+           |          |
|                | TMDSn- = BTMDSn-           |          |
|                | TMDSCLK+ = BTMDSCLK+       | TMDSn+   |
|                | TMDSCLK- = BTMDSCLK-       | TMDSn-   |
|                | ATMDSn+ = High Impedance   | TMDSCLK+ |
|                | ATMDSCLK+ = High Impedance | TMDSCLK- |

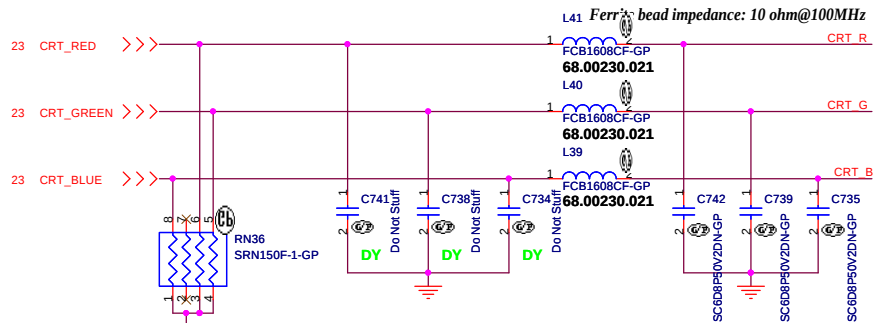


# LCD/INVERTER/CCD CONN



|                                                                                       |                            |                                                                                                             |          |
|---------------------------------------------------------------------------------------|----------------------------|-------------------------------------------------------------------------------------------------------------|----------|
| Pre UMA                                                                               |                            |                                                                                                             |          |
|  |                            | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |          |
| Title                                                                                 |                            |                                                                                                             |          |
| <b>LCD CONN</b>                                                                       |                            |                                                                                                             |          |
| Size                                                                                  | Document Number            |                                                                                                             | Rev      |
| <b>JE70-CP</b>                                                                        |                            | <b>-1M</b>                                                                                                  |          |
| Date:                                                                                 | Tuesday, February 02, 2010 | Sheet                                                                                                       | 24 of 67 |

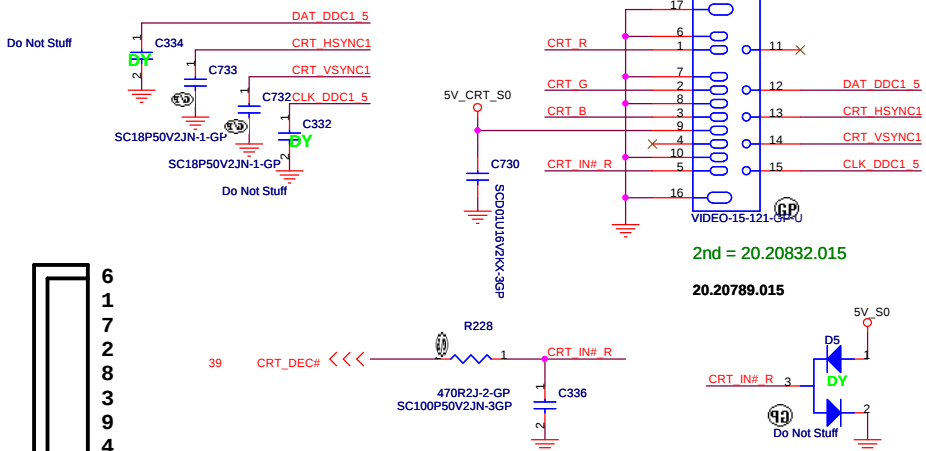
Layout Note:  
Place these resistors  
close to the CRT-out  
connector



#### Layout Note:

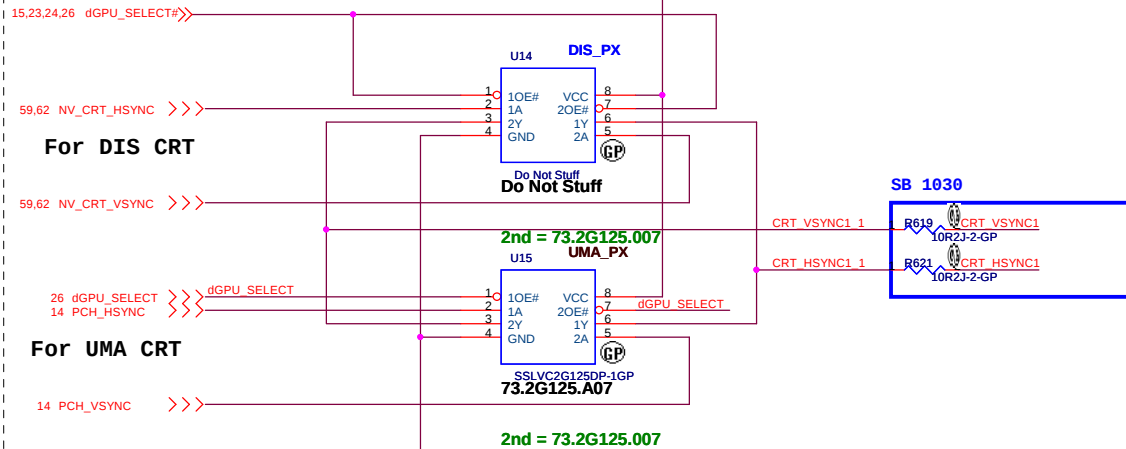
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

## CRT I/F & CONNECTOR

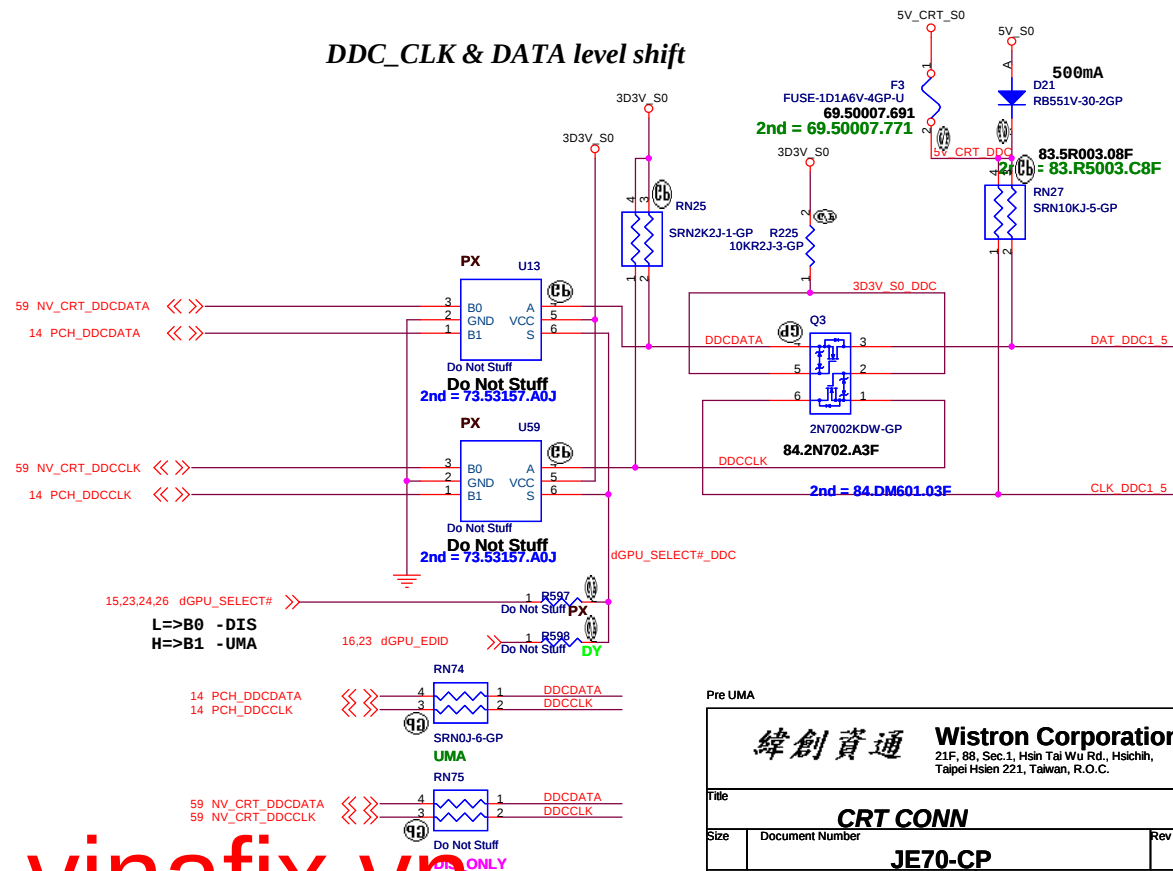


L=>B0 -DIS  
H=>B1 -UMA

### Hsync & Vsync level shift



### DDC\_CLK & DATA level shift

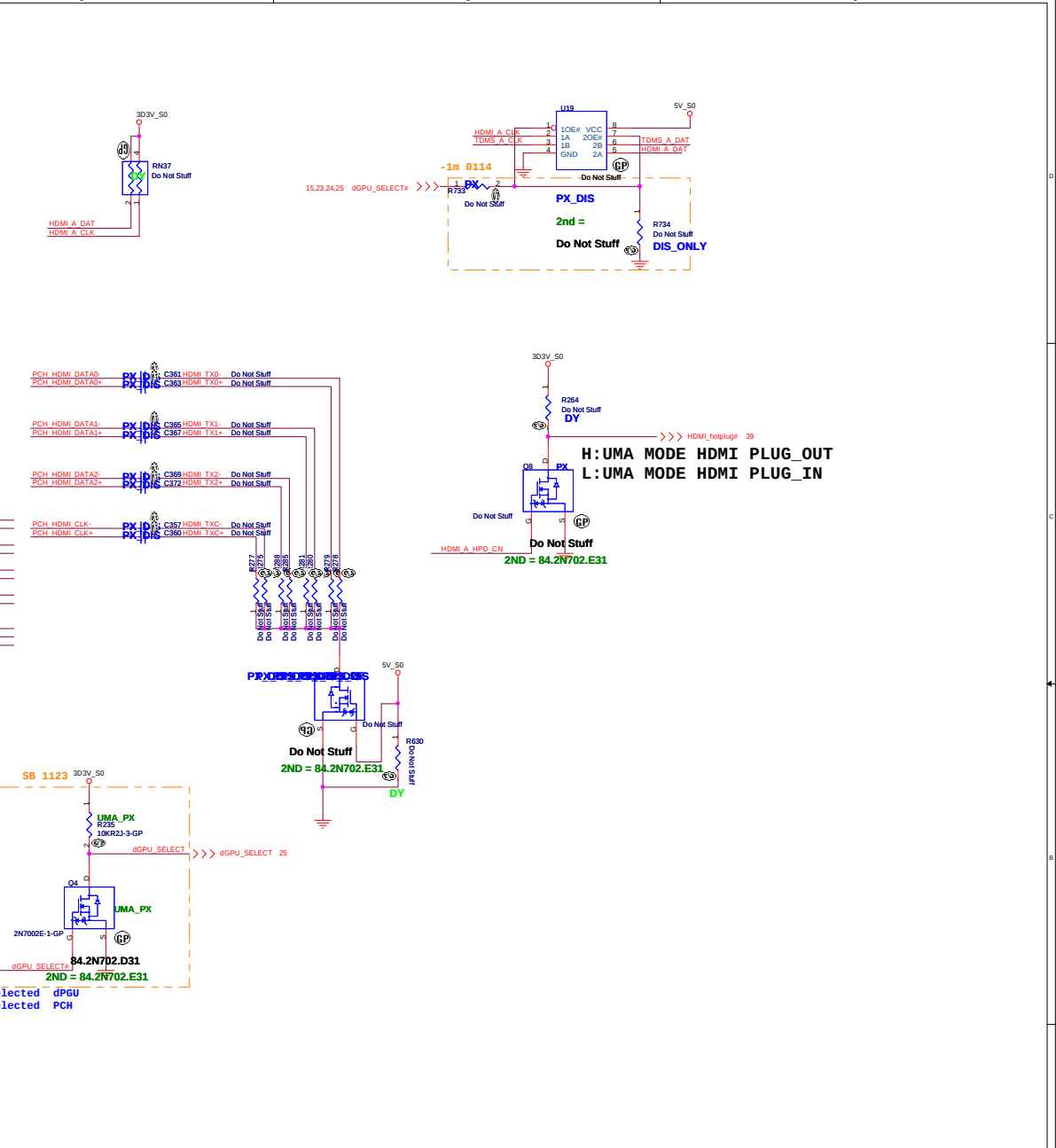
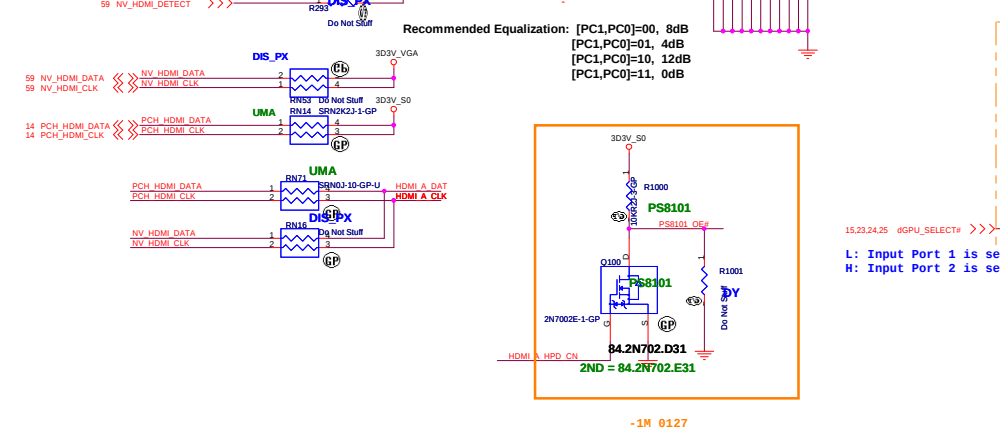


Pre UMA

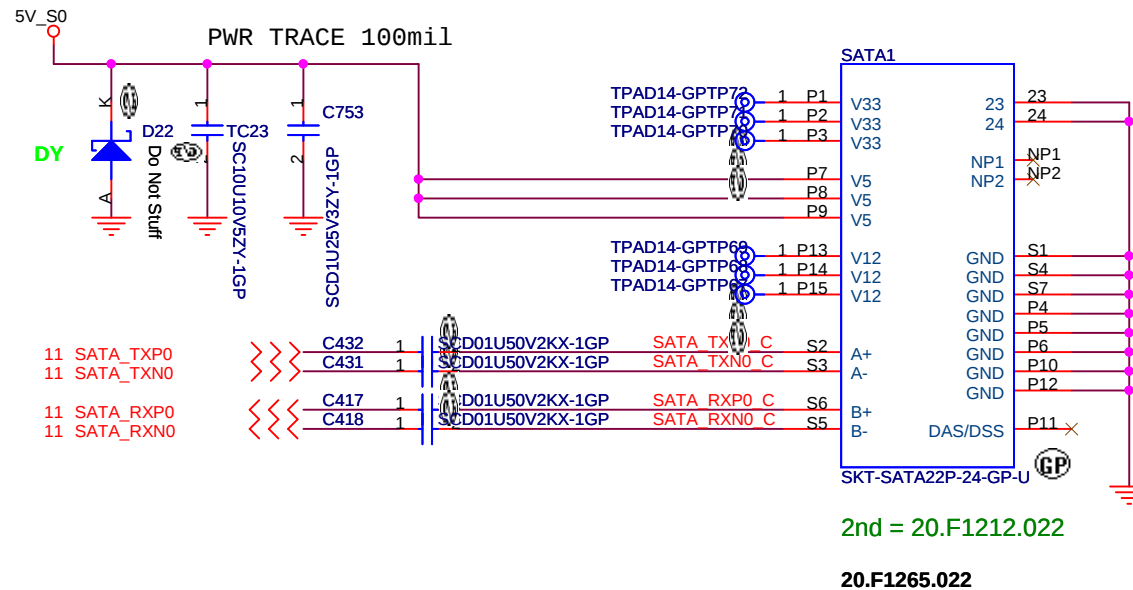
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

| Title                            |                 |     |
|----------------------------------|-----------------|-----|
| CRT CONN                         |                 |     |
| Size                             | Document Number | Rev |
|                                  | JE70-CP         | -1M |
| Date: Tuesday, February 02, 2010 | Sheet 25 of 67  |     |

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[illegible]

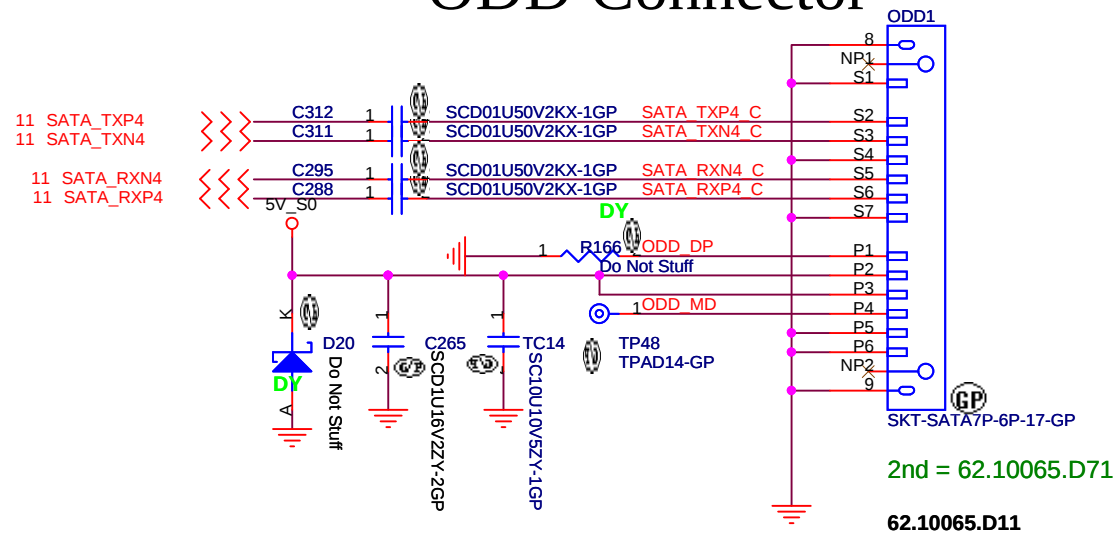
# SATA Connector



Pre UMA

|                 |                            |                                                                                                             |            |
|-----------------|----------------------------|-------------------------------------------------------------------------------------------------------------|------------|
| <b>緯創資通</b>     |                            | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |            |
| Title           |                            |                                                                                                             |            |
| <b>HDD CONN</b> |                            |                                                                                                             |            |
| Size            | Document Number            |                                                                                                             | Rev        |
|                 | <b>JE70-CP</b>             |                                                                                                             | <b>-1M</b> |
| Date:           | Tuesday, February 02, 2010 | Sheet                                                                                                       | 27 of 67   |

# ODD Connector



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Title

**ODD**

Size

Document Number

**JE70-CP**

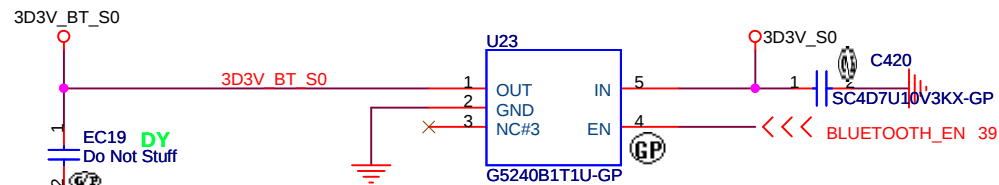
Rev

-1M

Date: Tuesday, February 02, 2010

Sheet 28 of 67

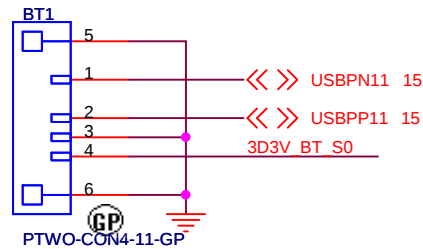
# BLUETOOTH MODULE



74.05240.A7F

2nd = 74.09711.A7F

EC20 put near  
BLUE1 / all  
USB put one  
choke near  
connector by  
EMI request



20.F1561.004

2nd = 20.F1621.004

Pre UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**BLUETOOTH**

Size

Document Number

**JE70-CP**

Rev

-1M

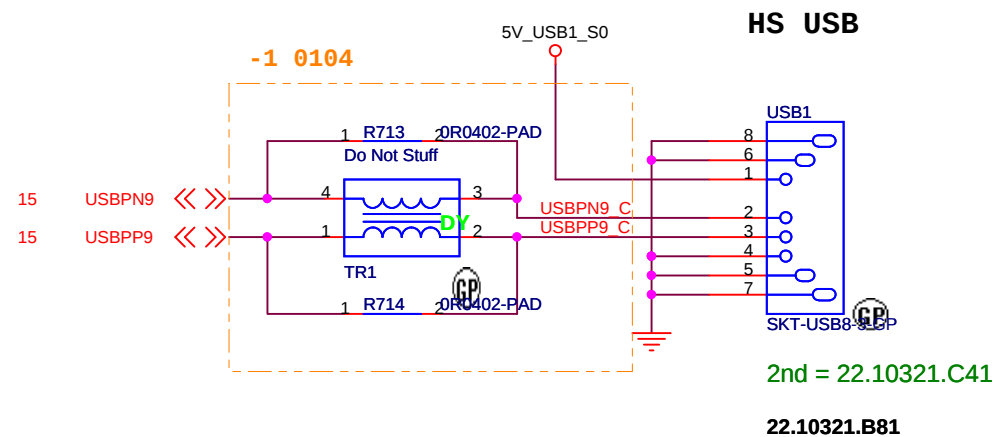
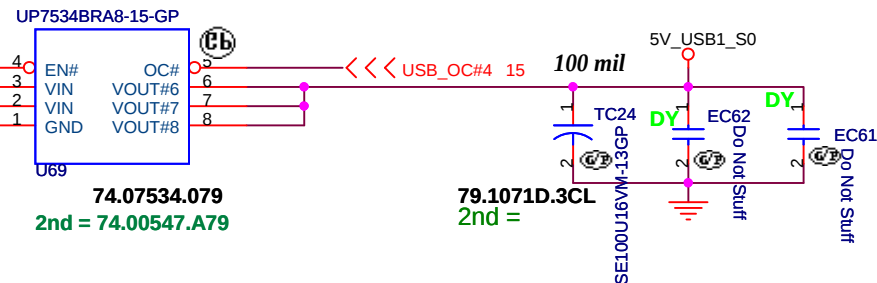
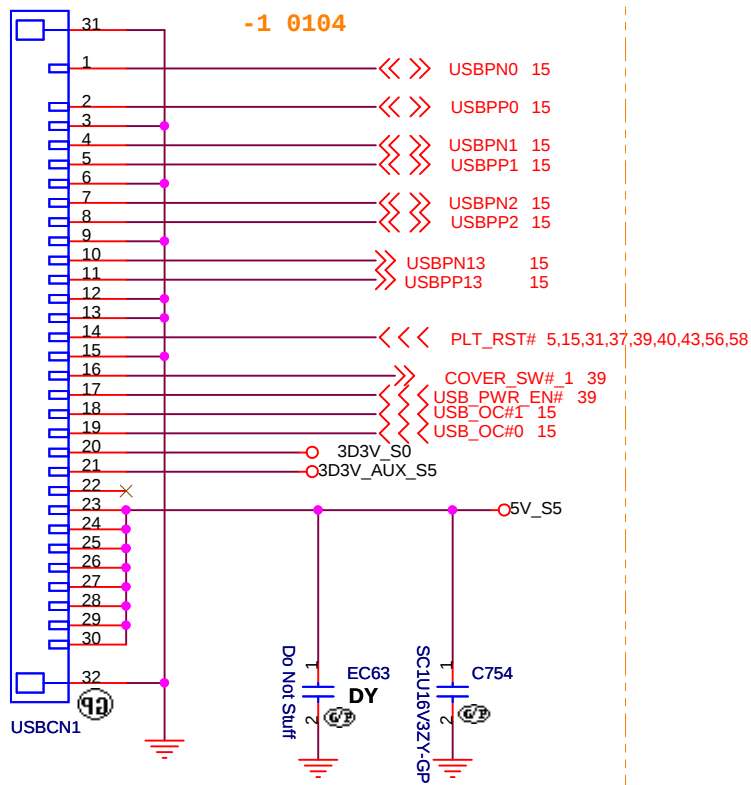
Date: Tuesday, February 02, 2010

Sheet 29 of 67

2nd =

20.K0276.030

ACES-CON30-4-GP-U



Pre UMA

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Title

USB CONN

Size

Document Number

JE70-CP

Rev

-1M

Date: Tuesday, February 02, 2010

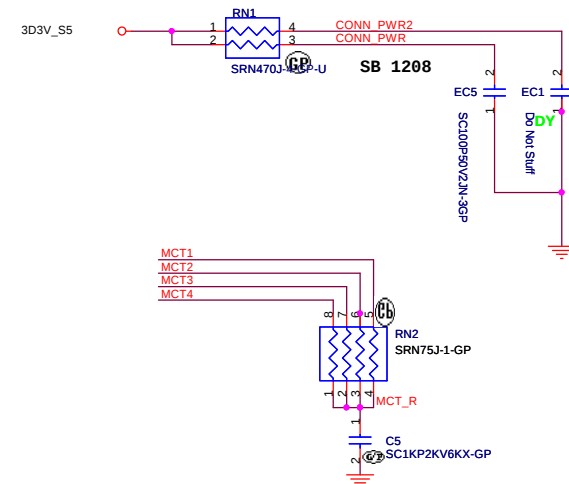
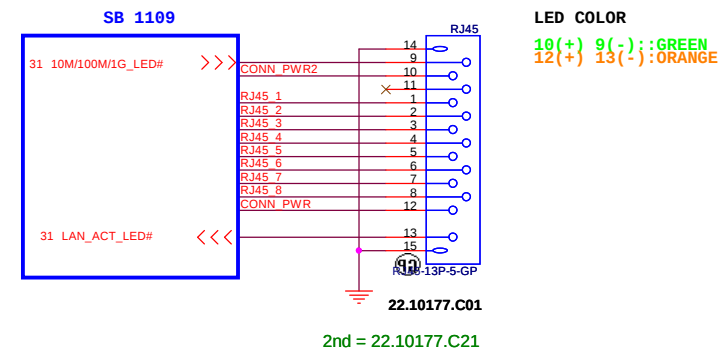
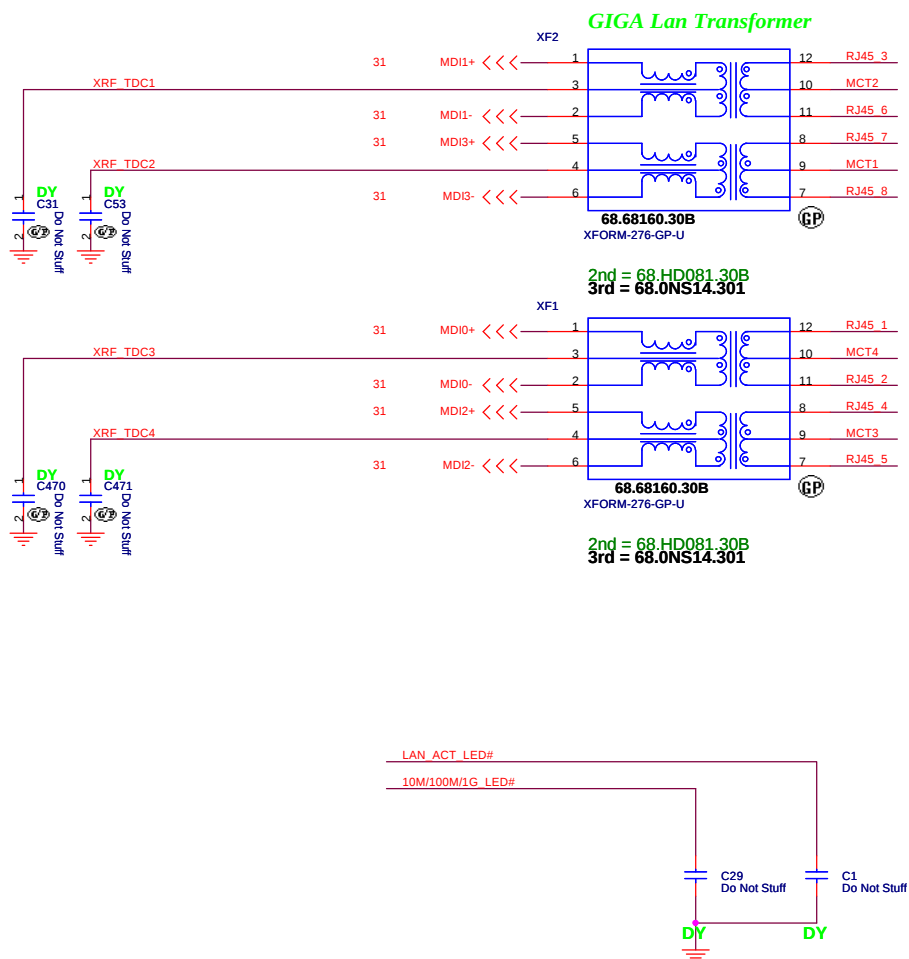
Sheet 30 of 67



# LAN Connector

# LAN Connector

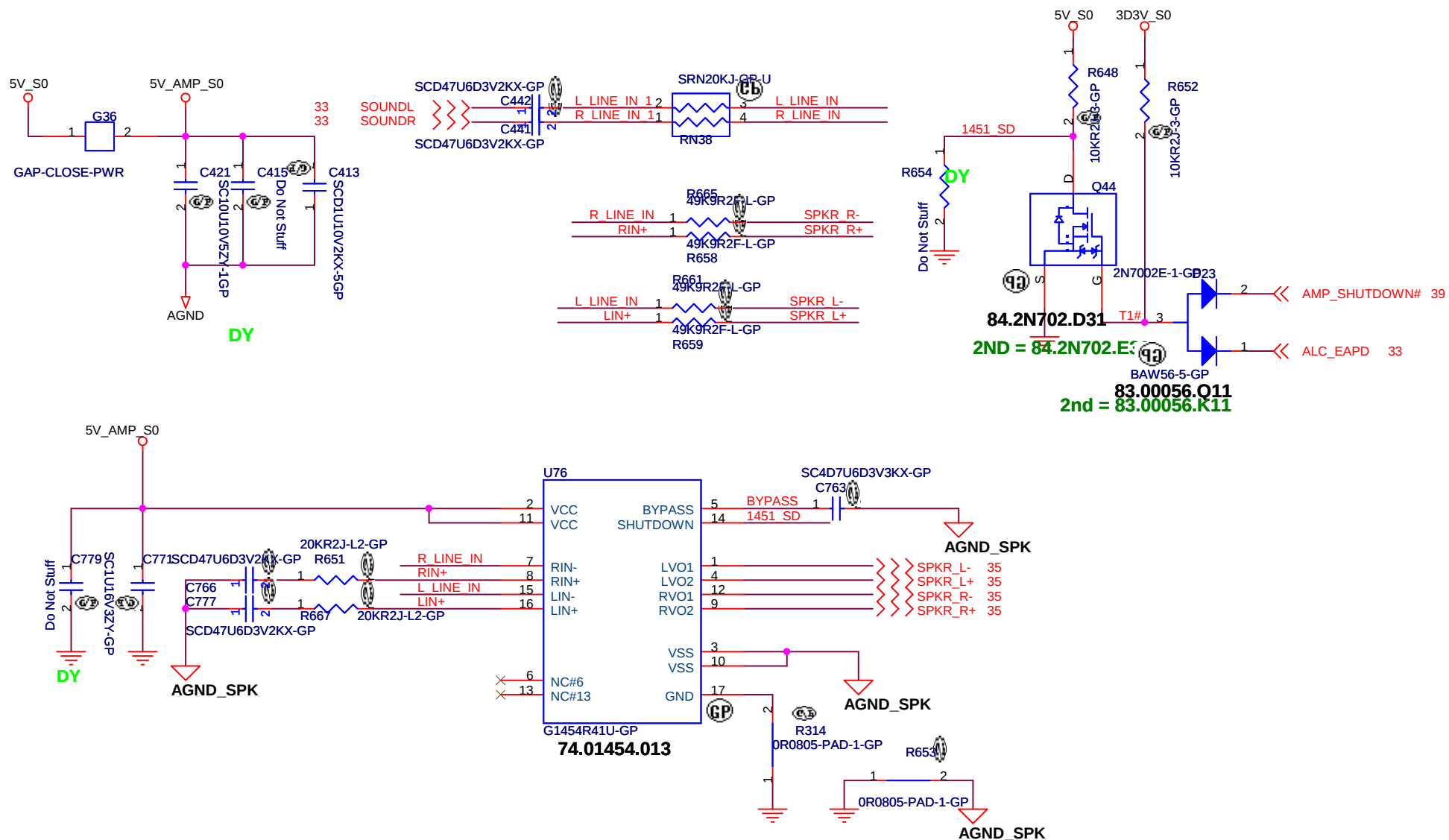
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



|                                  |                                   |                                                                                                                  |  |
|----------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------|--|
| Pre UMA                          |                                   | <b>緯創資通</b> Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |  |
| Title                            |                                   | <b>LAN CONN</b>                                                                                                  |  |
| Size<br>A3                       | Document Number<br><b>JE70-CP</b> | Rev<br><b>-1M</b>                                                                                                |  |
| Date: Tuesday, February 02, 2010 | Sheet 32 of 67                    |                                                                                                                  |  |



# AUDIO OP AMPLIFIER



Pre UMA

緯創資通

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Title

**AUDIO AMP**

Size

Document Number

**JE70-CP**

Rev

**-1M**

Date: Tuesday, February 02, 2010

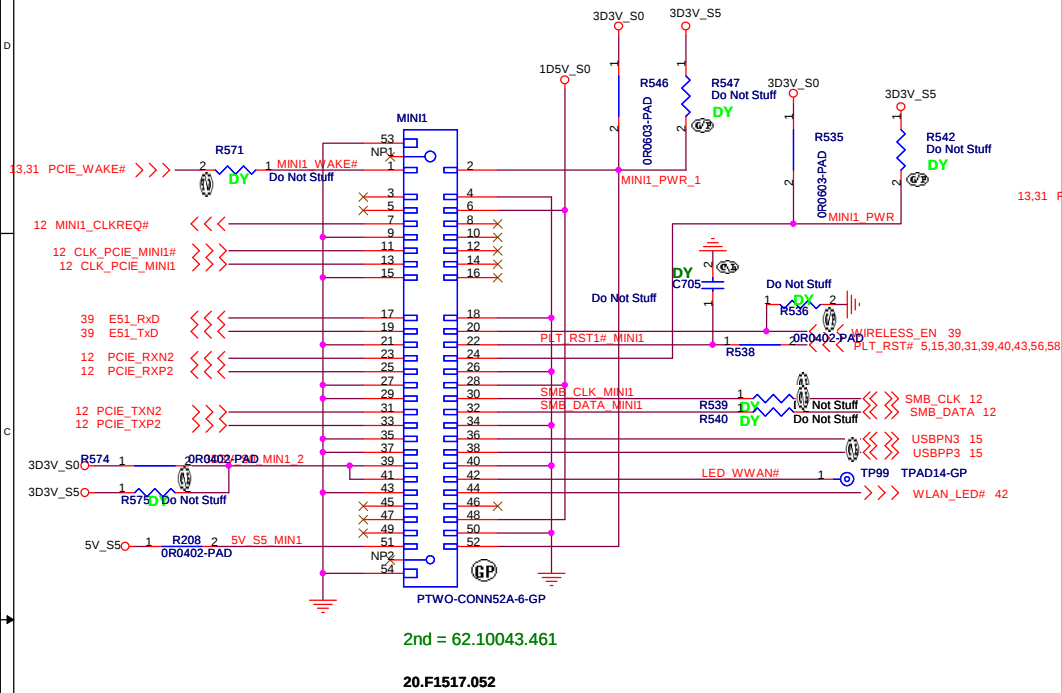
Sheet 34 of 67

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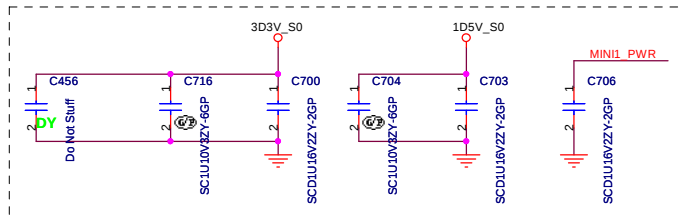
## ***Mini Card Connector(WLAN) Support debug-card***



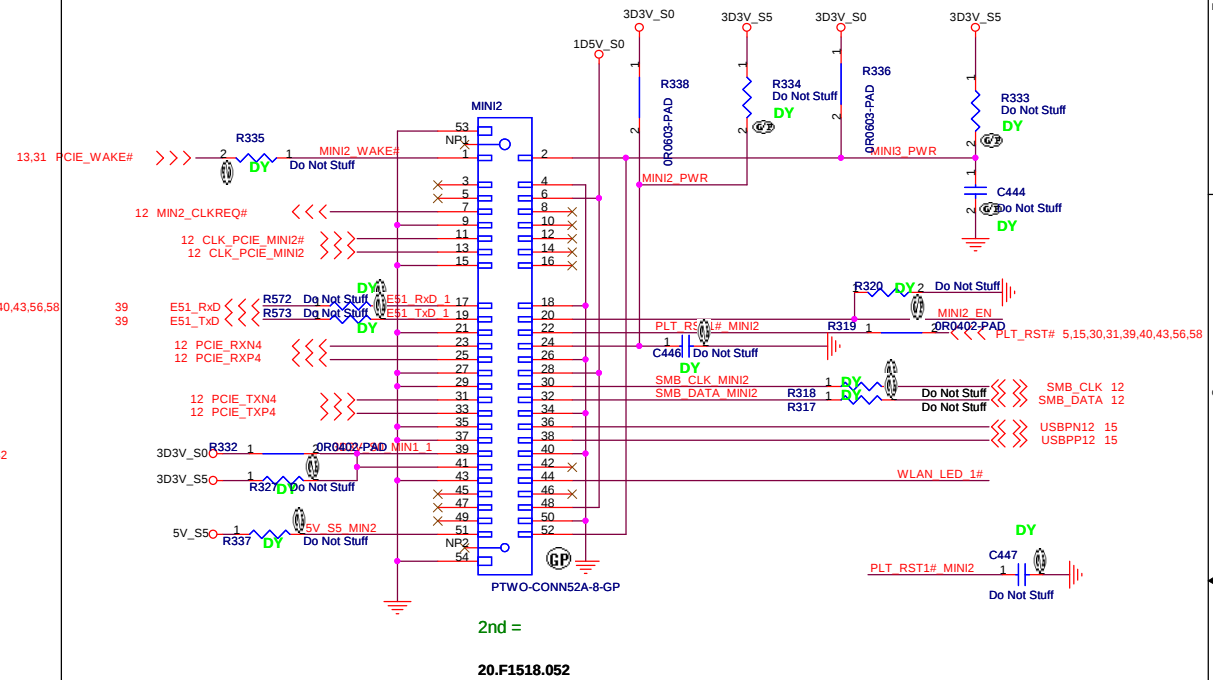
2nd = 62.10043.461

**20.F1517.052**

Place near MINI1



### ***Mini Card Connector(Robson2 and 3G)***

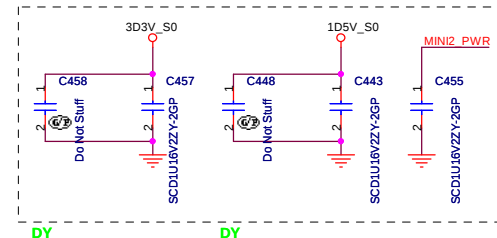


2nd =

**20.F1518.052**

WLAN\_LED# R534 Do Not Stuff WLAN\_LED\_1#  
WIRELESS\_EN 1 Do Not Stuff MINI2\_EN  
R537

Place near MINIC2



Pre UMA

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| Title |
|-------|
|-------|

**MINI CARD**

Size

|  |                 |
|--|-----------------|
|  | Document Number |
|--|-----------------|

**JE70-CP**

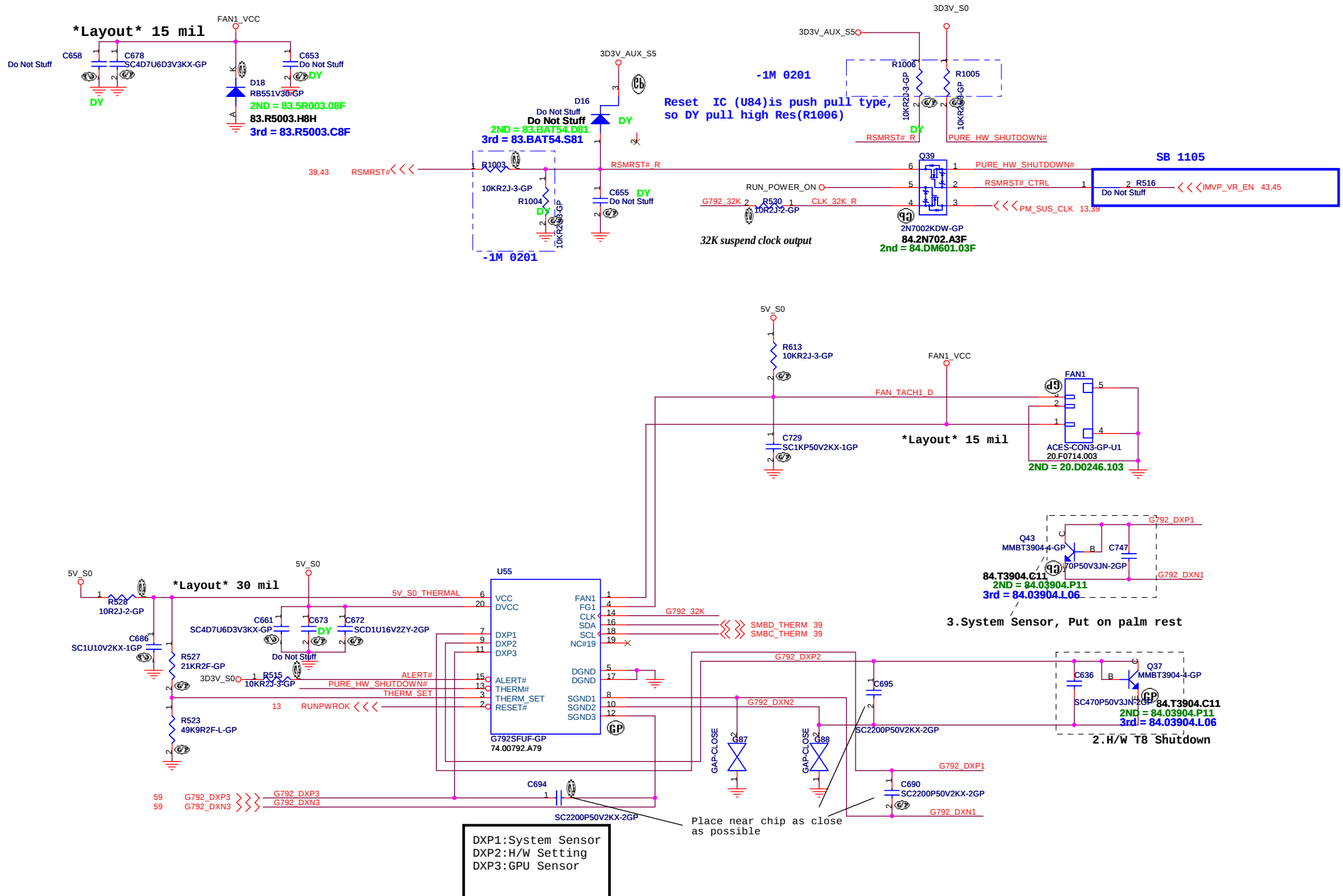
Date: Tuesday, February 02, 2010

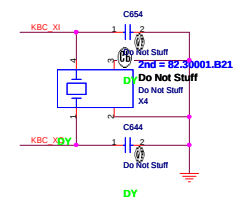
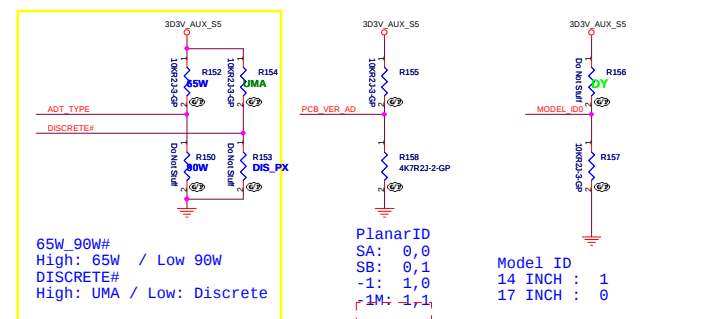
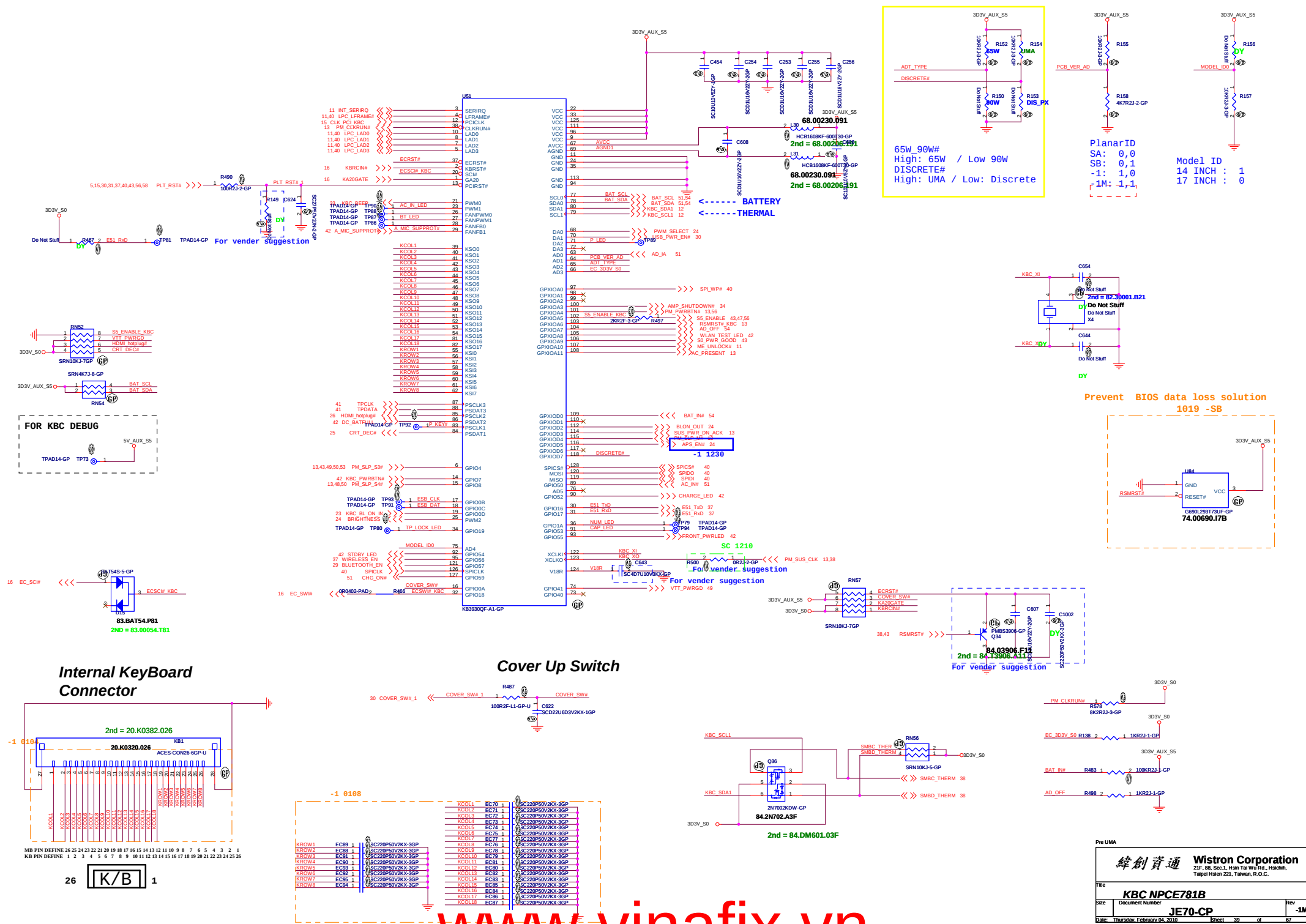
Sheet 37 of 67

|     |  |
|-----|--|
| Rev |  |
|-----|--|

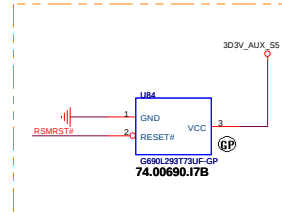
**-1M**

67

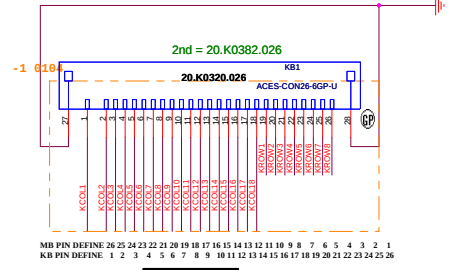




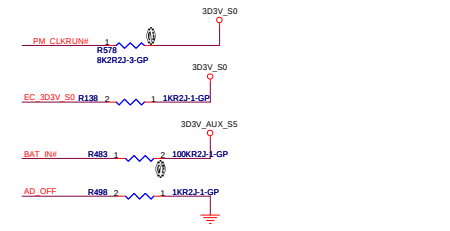
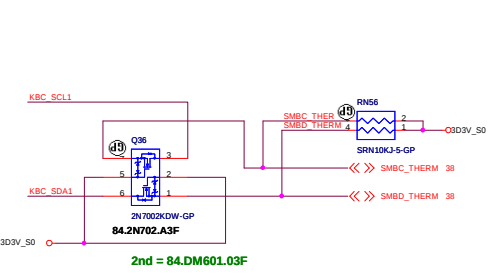
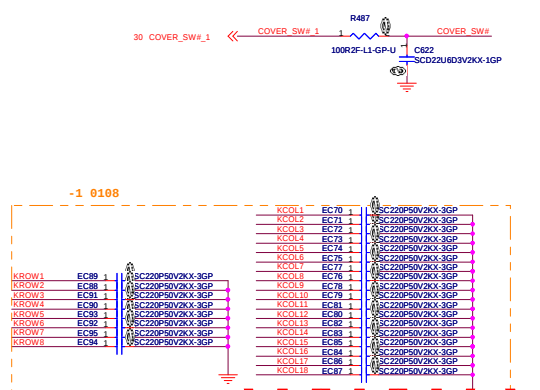
Prevent BIOS data loss solution  
1019 -SB



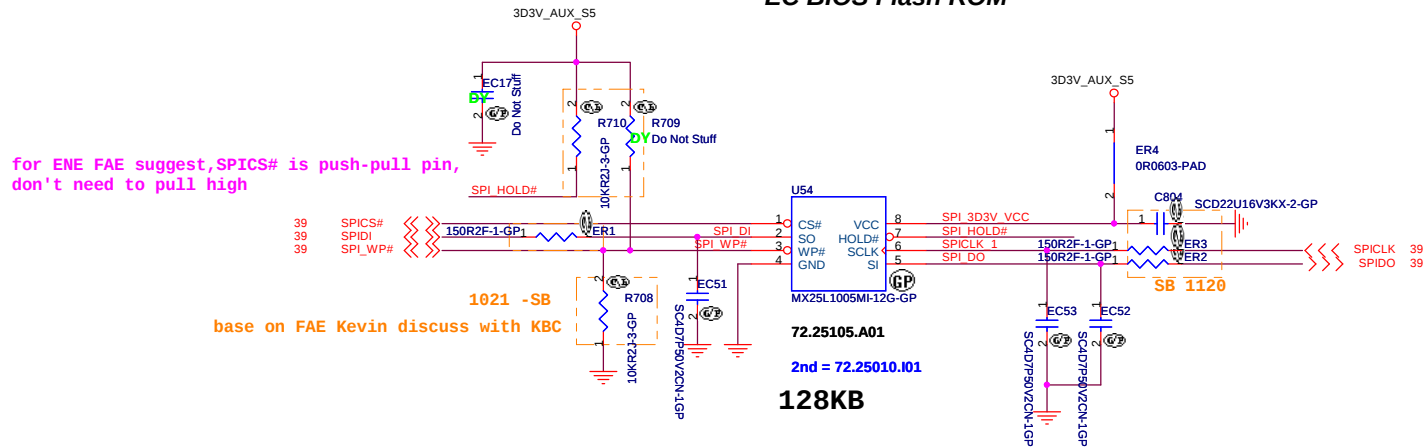
### Internal KeyBoard Connector



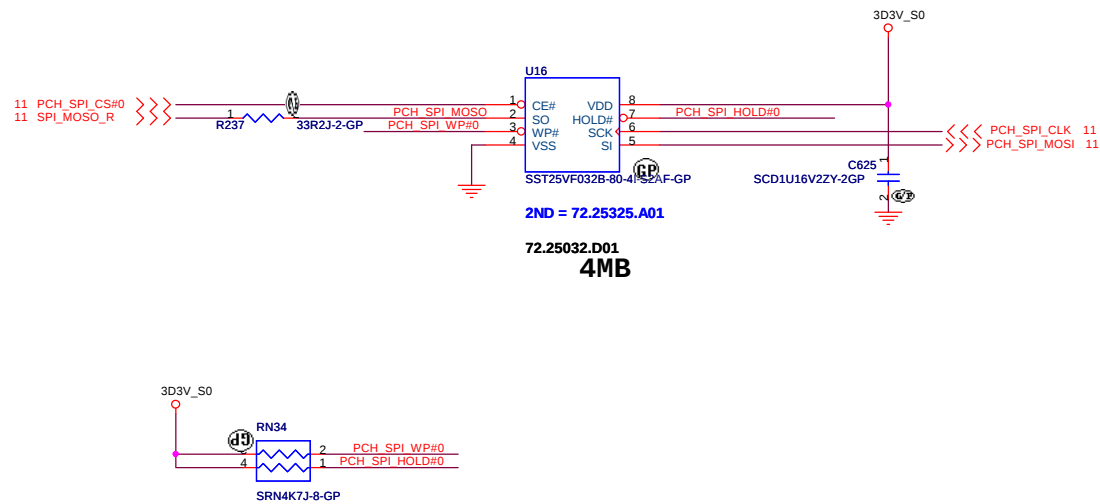
### Cover Up Switch



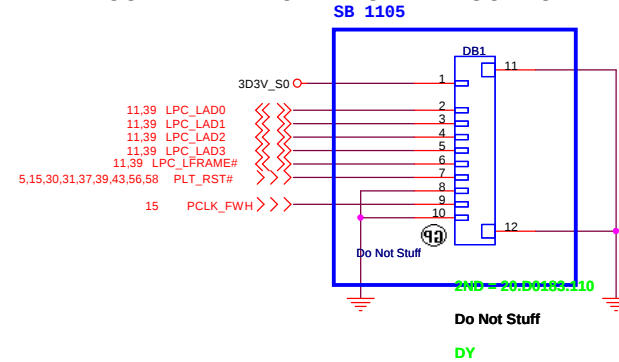
### EC BIOS Flash ROM



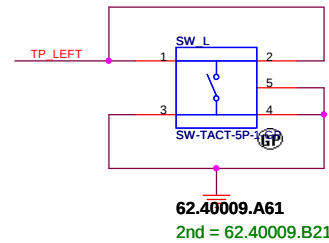
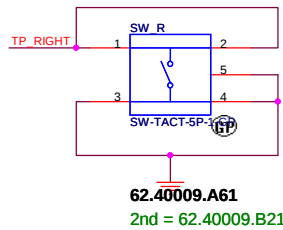
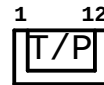
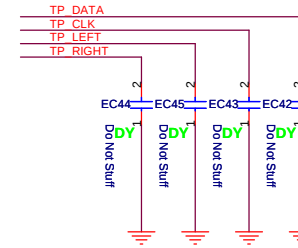
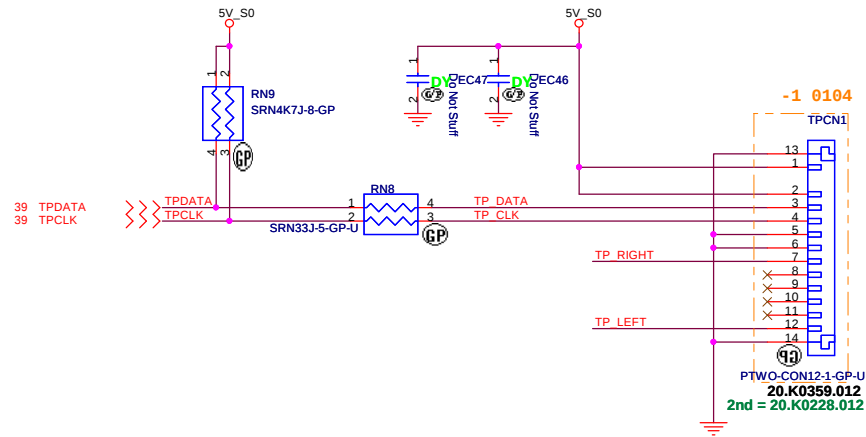
### System BIOS Flash ROM



## GOLDEN FINGER FOR DEBUG BOARD



# TOUCH PAD



Pre UMA

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Title

Touch PAD and FP

Size

Document Number

JE70-CP

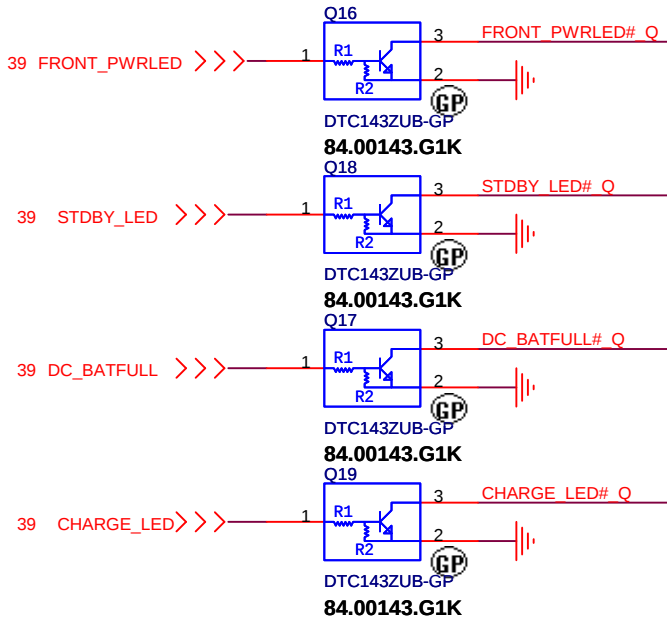
Rev

-1M

Date: Tuesday, February 02, 2010

Sheet 41 of 67

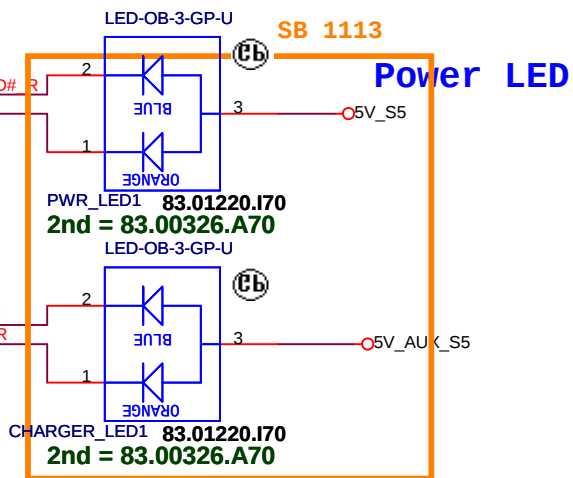
# LED



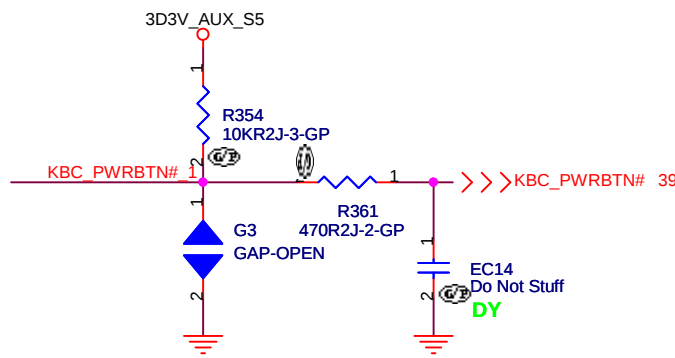
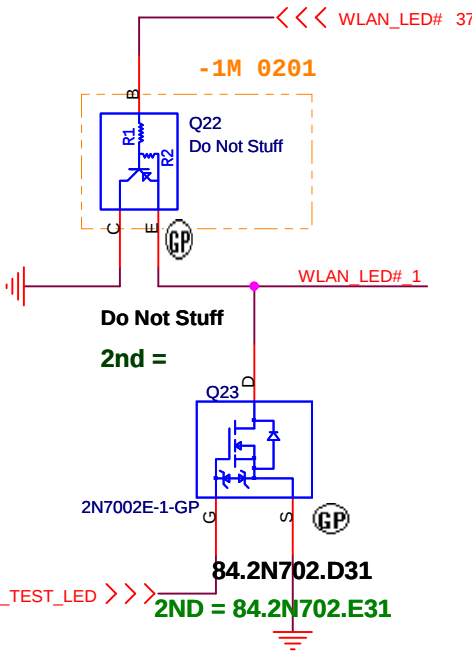
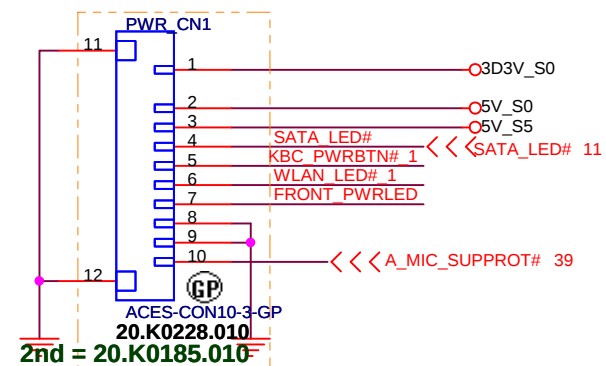
FRONT\_PWRLED# Q 1 R340 330R2F-GP  
STDBY\_LED# Q 1 R343 330R2F-GP  
DC\_BATFULL# Q 1 R341 330R2F-GP  
CHARGE\_LED# Q 1 R344 330R2F-GP

FRONT\_PWRLED# Q 1 DY EC22 Do Not Stuff  
CHARGE\_LED# Q 1 DY EC25 Do Not Stuff  
STDBY\_LED# Q 1 DY EC24 Do Not Stuff  
DC\_BATFULL# Q 1 DY EC23 Do Not Stuff

-1 0107



-1 0104



SATA\_LED# EC34 2 DY Do Not Stuff  
KBC\_PWRBTN# 1 EC33 DY Do Not Stuff  
WLAN\_LED# 1 EC35 DY Do Not Stuff  
FRONT\_PWRLED EC36 DY Do Not Stuff

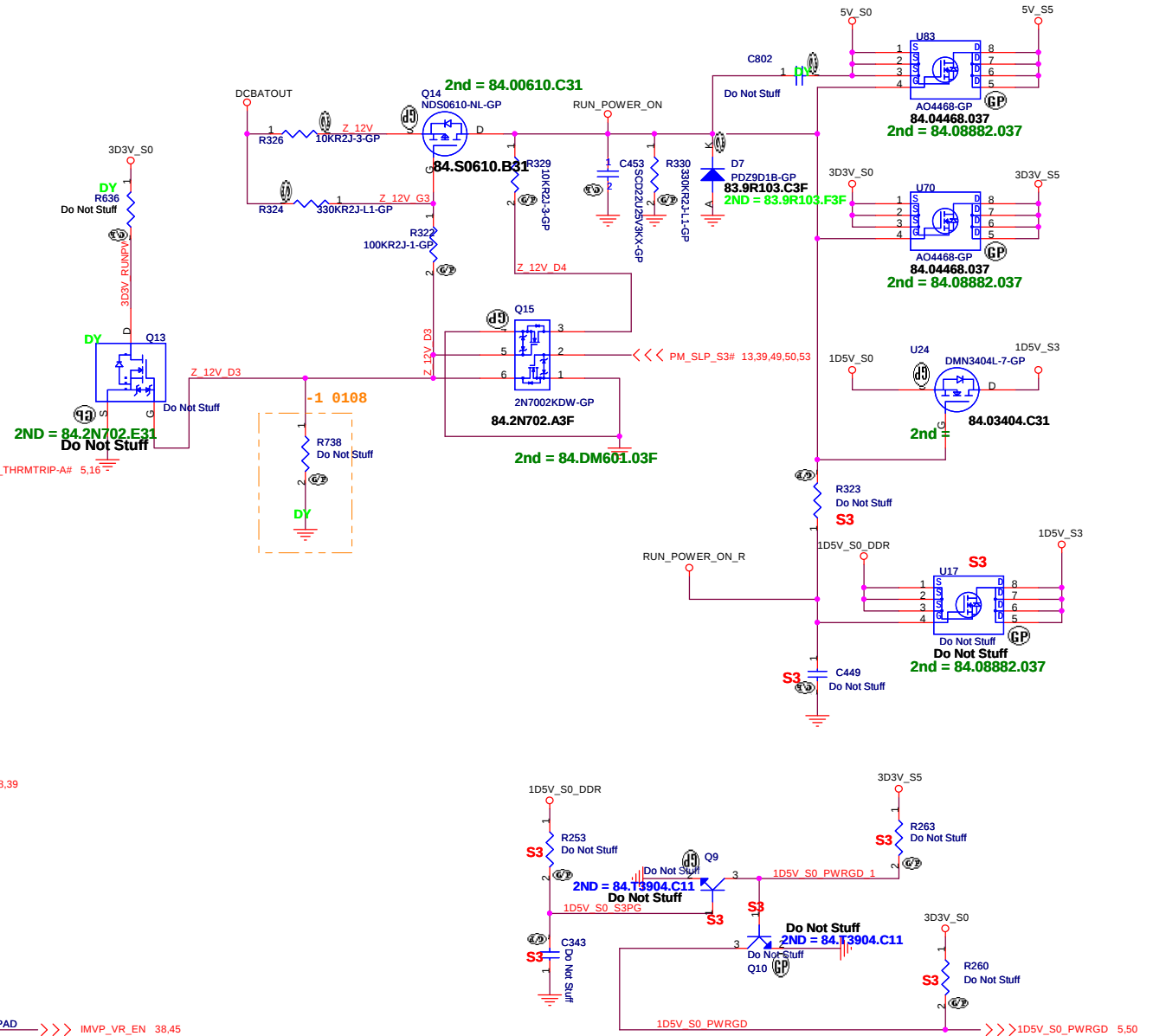
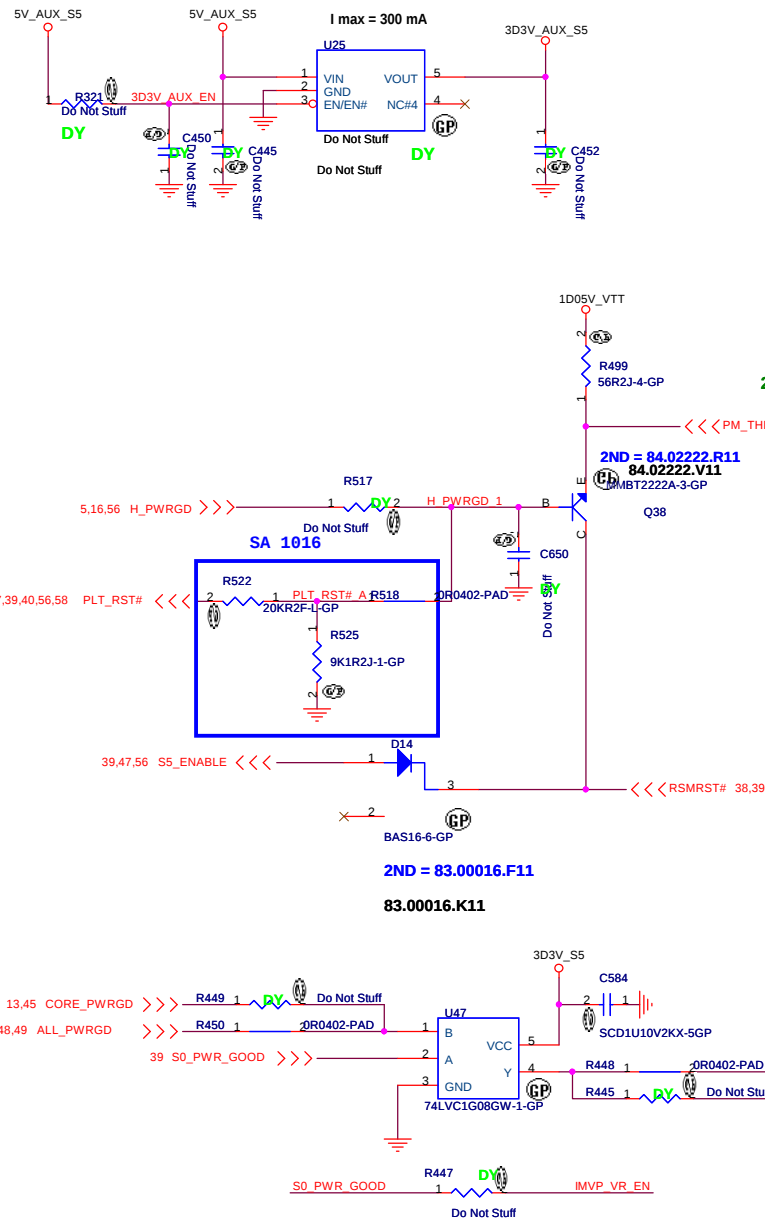
Pre UMA

|                                                                                                                         |                 |
|-------------------------------------------------------------------------------------------------------------------------|-----------------|
| <b>緯創資通</b> <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                 |
| Title                                                                                                                   |                 |
| <b>LED&amp;POWERBD CONN</b>                                                                                             |                 |
| Size                                                                                                                    | Document Number |
| <b>JE70-CP</b>                                                                                                          |                 |
| Date: Tuesday, February 02, 2010                                                                                        | Sheet 42 of 67  |
| Rev -1M                                                                                                                 |                 |

## Run Power

### Aux Power

**3D3V\_AUX\_S5**



Pre UMA

緯創資通

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|  |       |
|--|-------|
|  | Title |
|--|-------|

### ***RUN POWER and 3D3V AUX S5***

Size

Document Number

**JE70-CP**

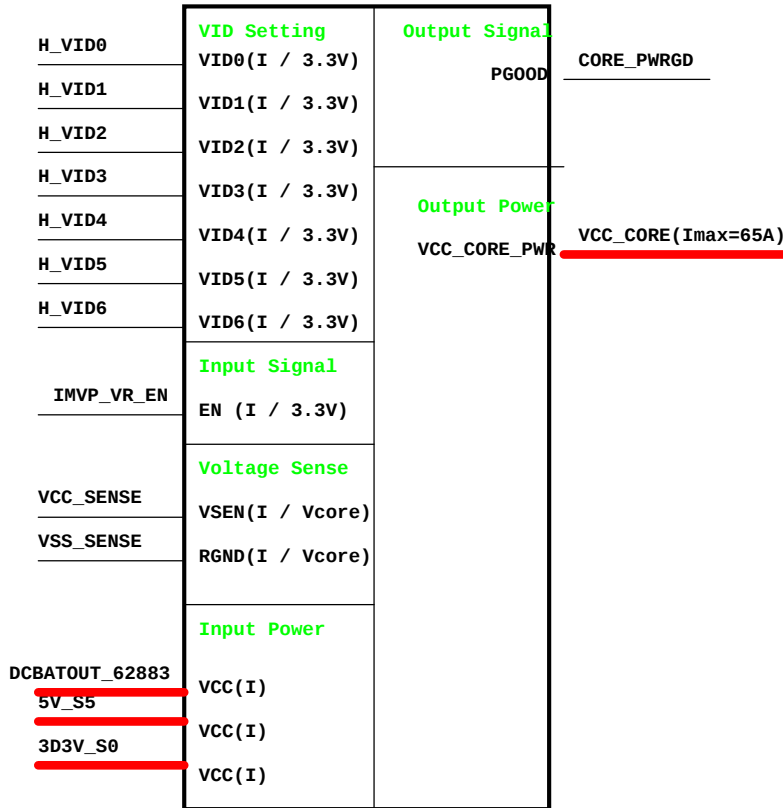
-1M

Date: Tuesday, February 02, 2010

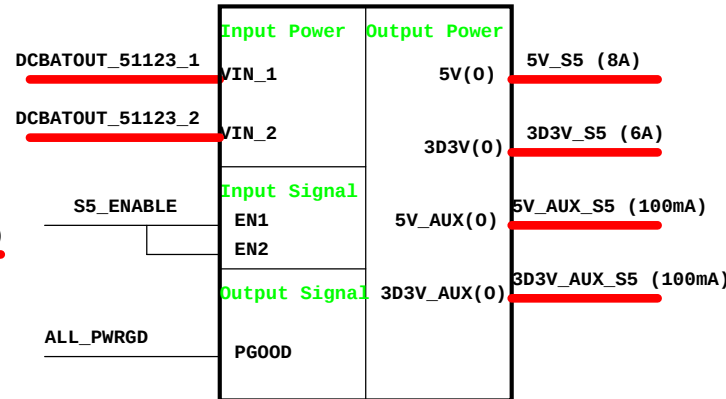
Sheet 43 of 67

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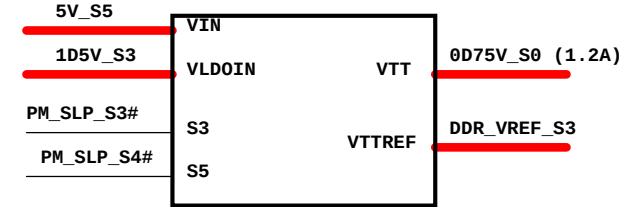
# ISL62883 VCC\_CORE



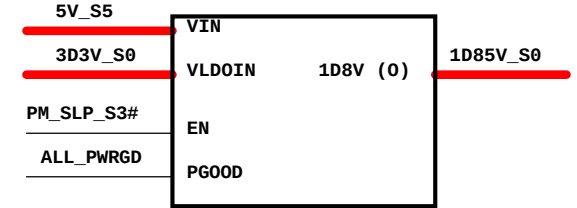
# TPS51123 5V/3D3V



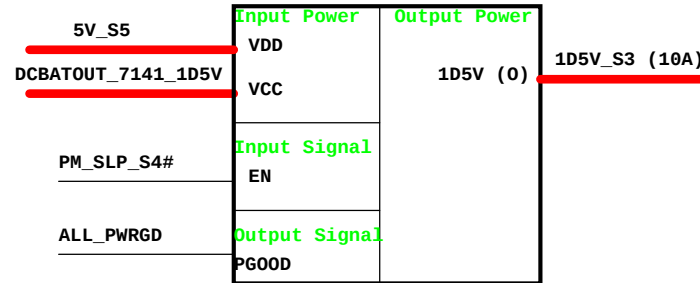
# RT9026 0D75V\_S0



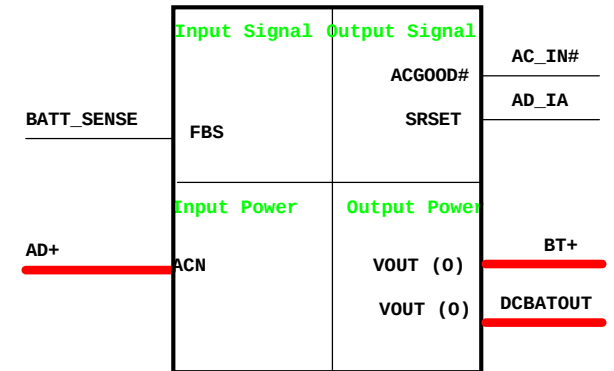
# RT9025 1D8V



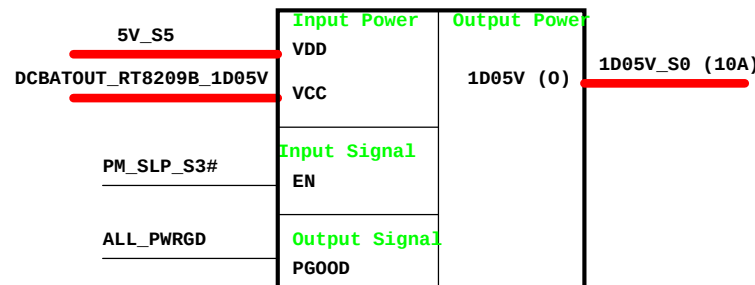
# RT9025 1D5V



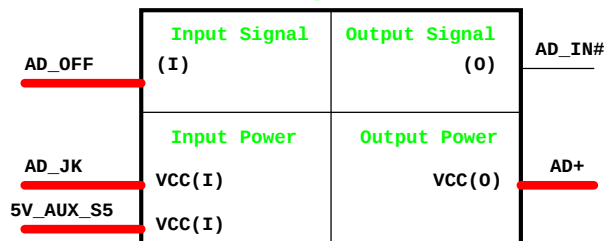
# Charger BQ24745



# RT8209B 1D05V



# Adapter



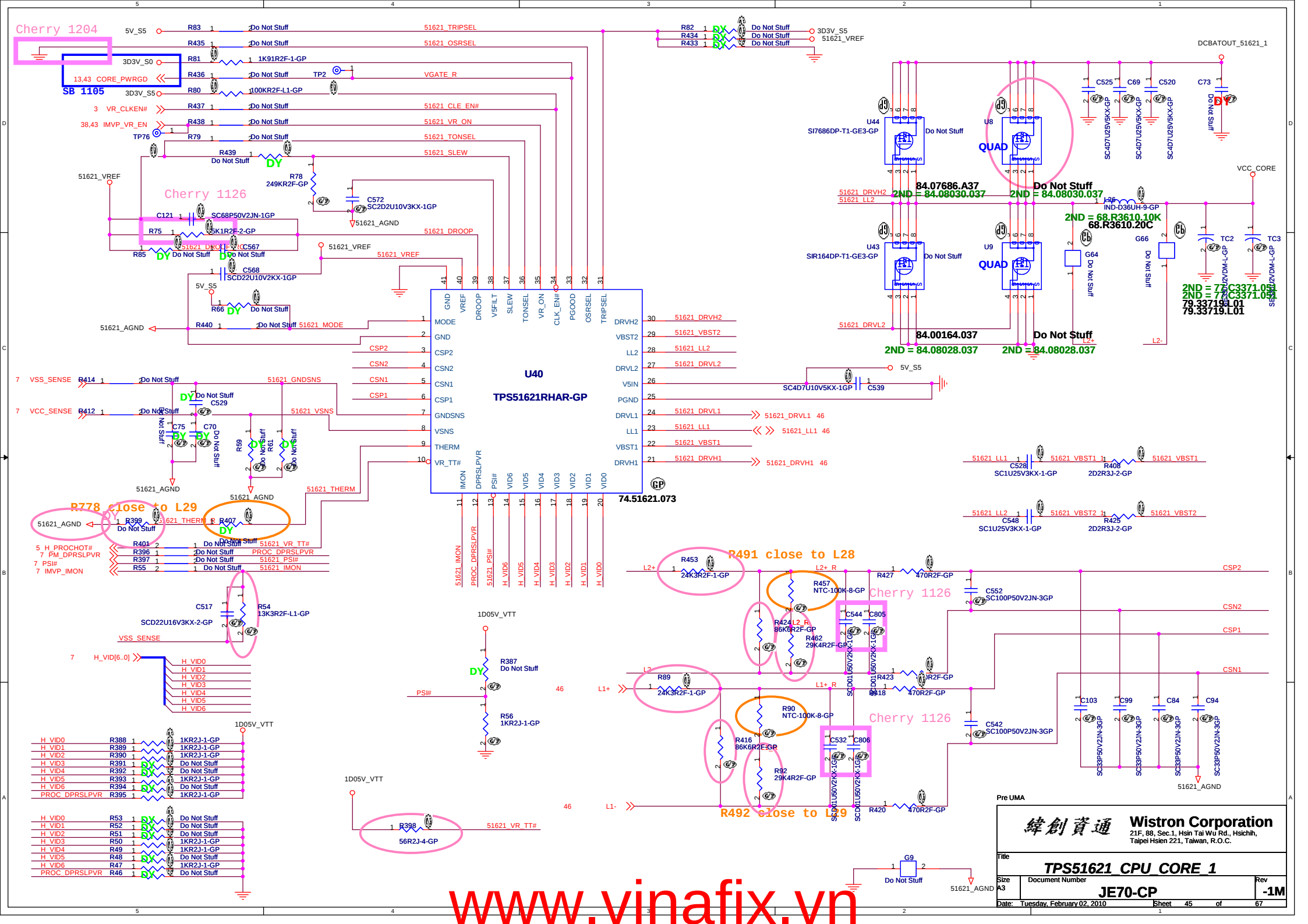
Pre UMA

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Title **Power Block Diagram**

Size Document Number **JE70-CP** Rev **-1M**

Date: Tuesday, February 02, 2010 Sheet 44 of 67



Cherry 1204

Cherry 1126

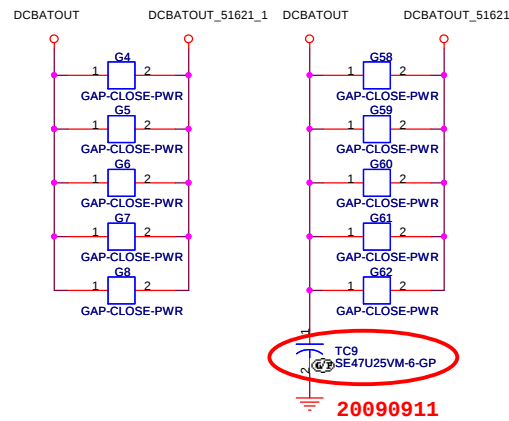
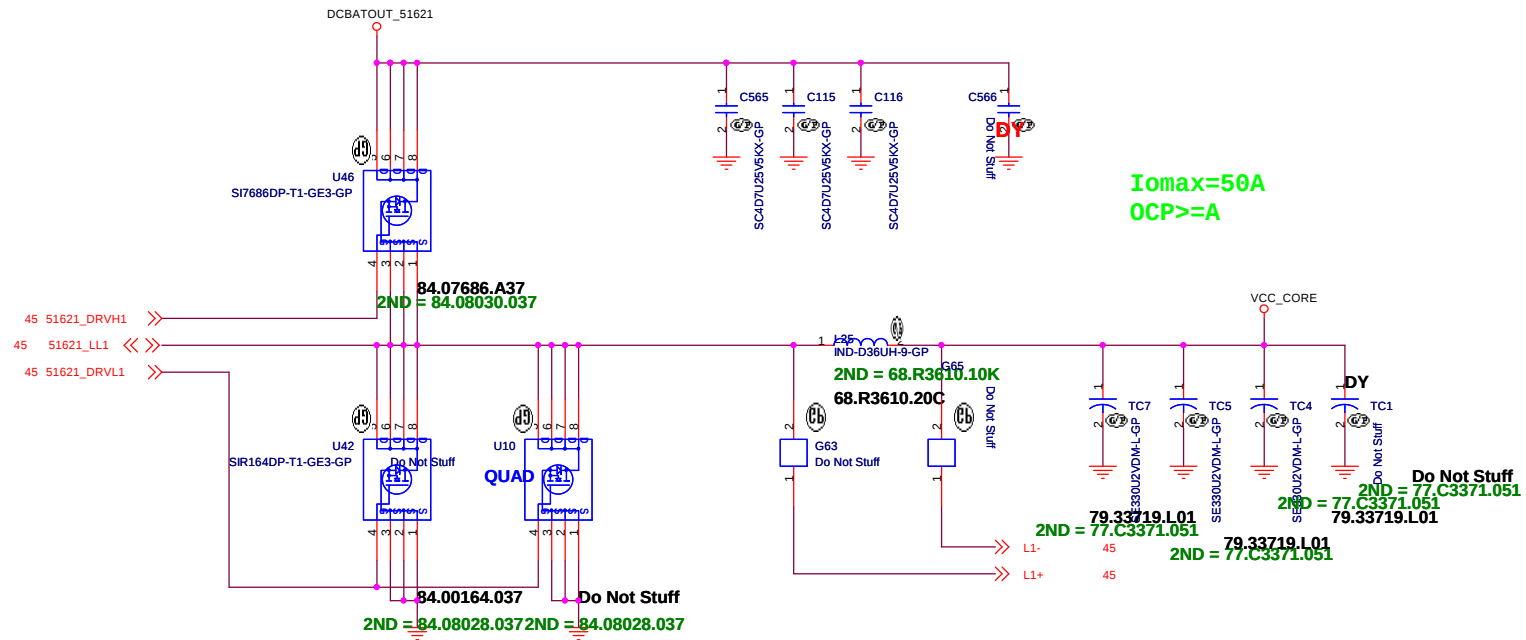
Cherry 1126

Cherry 1126

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Taipei Hsien 221, Taiwan, R.O.C.

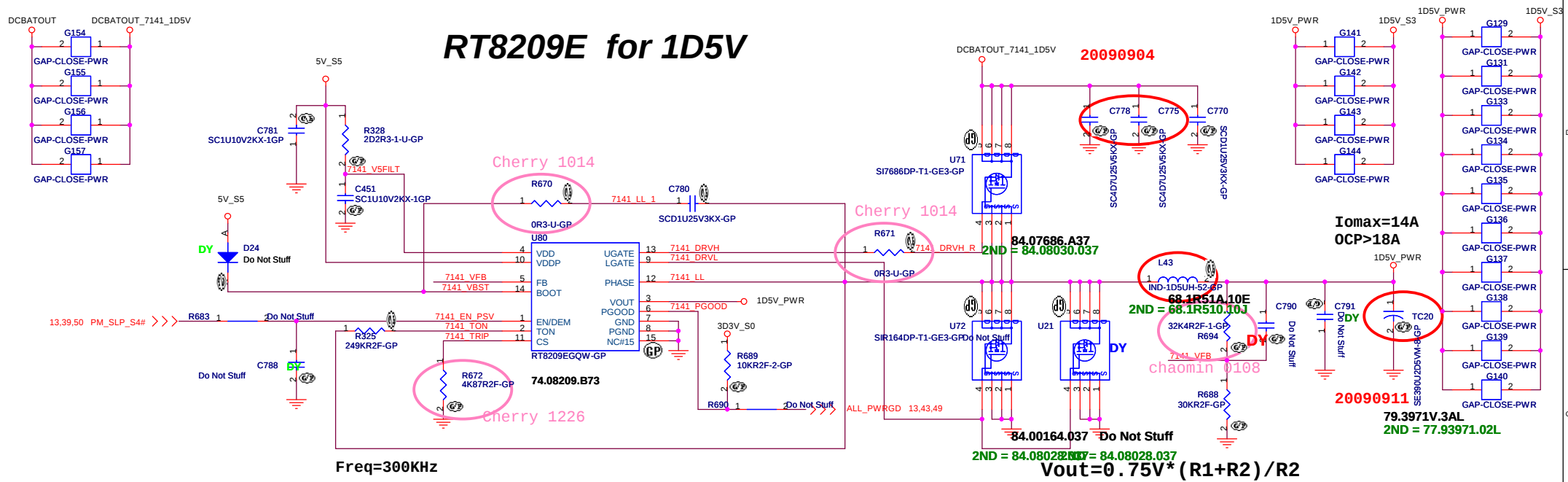
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|-------|----------------------------|-------|---------------------|
| Title |                            |       | TPS51621 CPU CORE 1 |
| Size  | Document Number            | Rev   | -1M                 |
| A3    | JE70-CP                    |       |                     |
| Date: | Tuesday, February 02, 2010 | Sheet | 45 of 67            |

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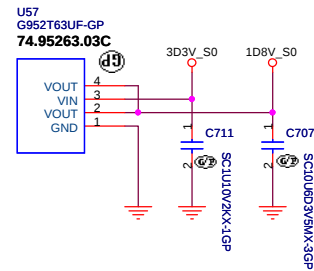


## RT8209E for 1D5V



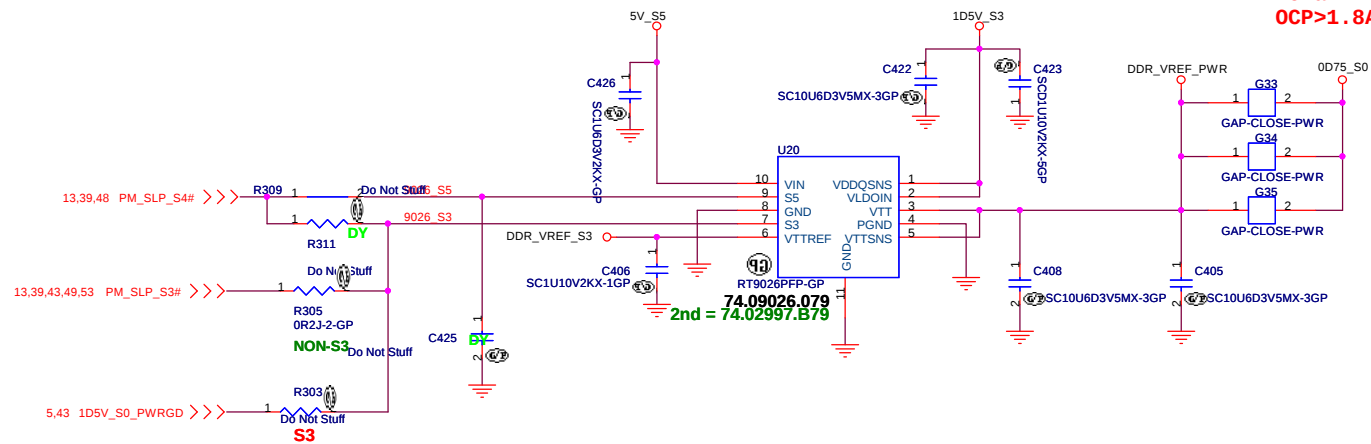


# 1.8V\_S0 1.8V 1A Regulator



## RT9026 for 0D75V\_S3

Iomax=1.2A  
OCP>1.8A



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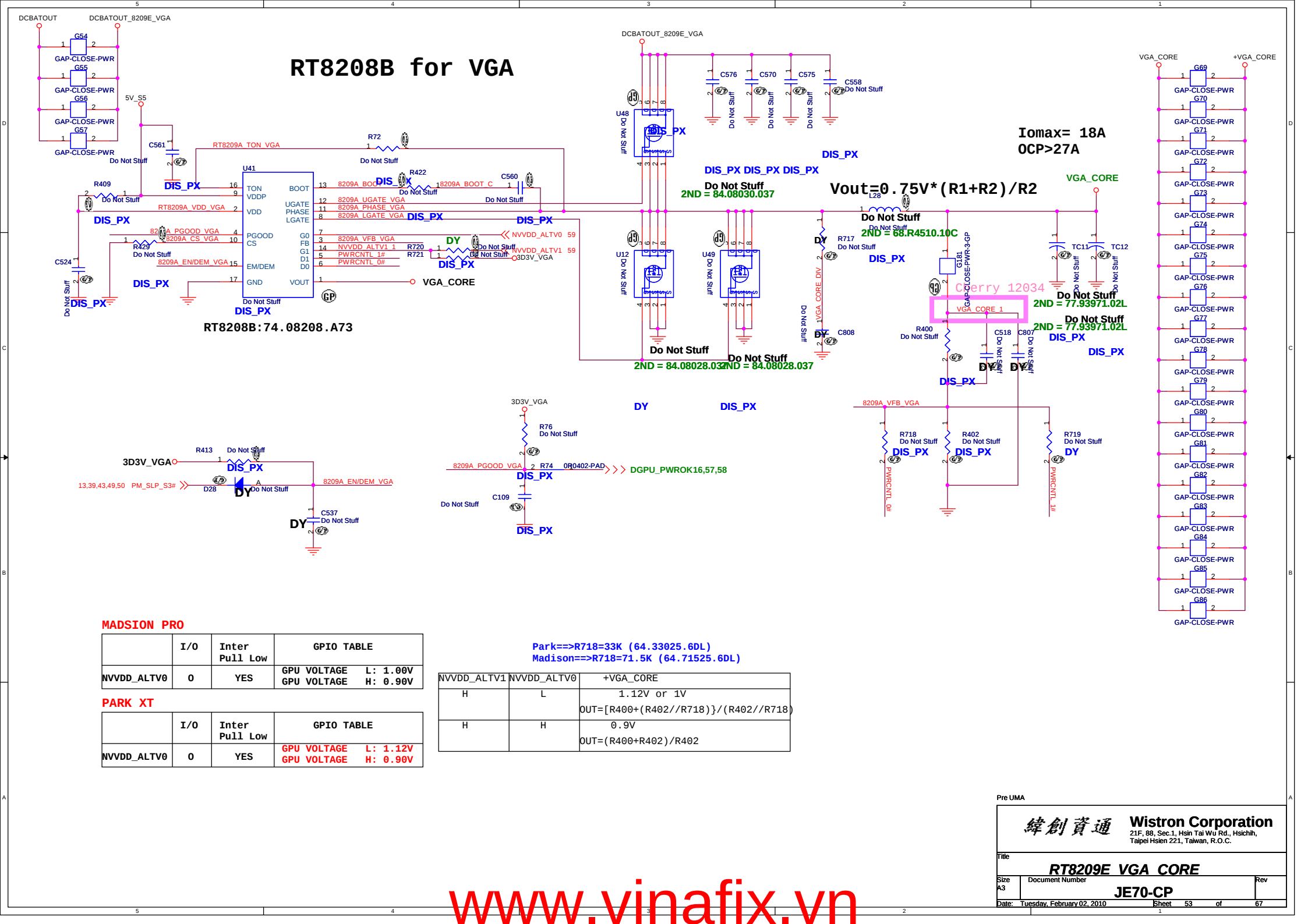
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| Title                        |                 | Rev                              |          |
| RT8015A for 1D8V/RT9026 0D75 |                 | -1M                              |          |
| Size                         | Document Number | Date: Tuesday, February 02, 2010 |          |
| JE70-CP                      |                 | Sheet                            | 50 of 67 |





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[illegible]

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**RT8208B for VGA**

**RT8208B: 74.08208.A73**

**MADSION PRO**

| I/O        | Inter Pull Low | GPIO TABLE                                    |
|------------|----------------|-----------------------------------------------|
| NVDD_ALTV0 | 0              | YES GPU VOLTAGE L: 1.00V GPU VOLTAGE H: 0.90V |

**PARK XT**

| I/O        | Inter Pull Low | GPIO TABLE                                    |
|------------|----------------|-----------------------------------------------|
| NVDD_ALTV0 | 0              | YES GPU VOLTAGE L: 1.12V GPU VOLTAGE H: 0.90V |

**Park==>R718=33K (64.33025.6DL)**  
**Madison==>R718=71.5K (64.71525.6DL)**

| NVDD_ALTV1 | NVDD_ALTV0 | +VGA_CORE                                           |
|------------|------------|-----------------------------------------------------|
| H          | L          | 1.12V or 1V<br>OUT=[R400+(R402//R718)]/(R402//R718) |
| H          | H          | 0.9V<br>OUT=(R400+R402)/R402                        |

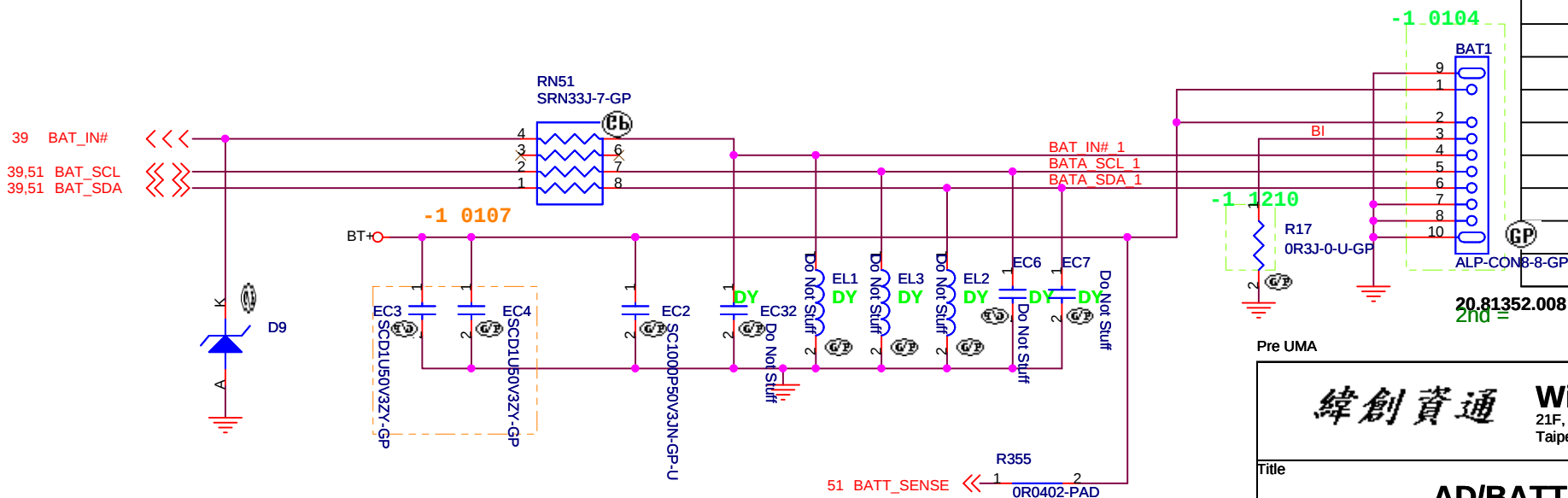
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**RT8209E VGA CORE**  
**JE70-CP**

Date: Tuesday, February 02, 2010 Sheet 53 of 67

[illegible]

## BATTERY CONNECTOR



| Pin NO | Symbol |
|--------|--------|
| 1      | GND    |
| 2      | GND    |
| 3      | SMD    |
| 4      | SMC    |
| 5      | TS     |
| 6      | B/I    |
| 7      | BT+    |
| 8      | BT+    |

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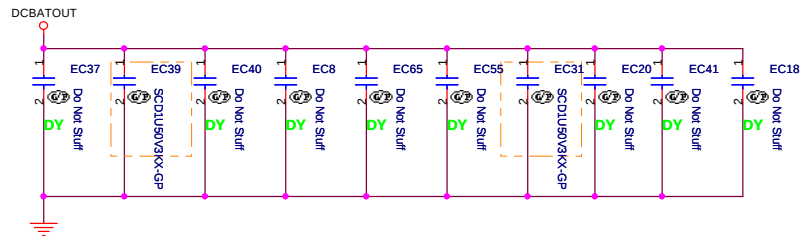
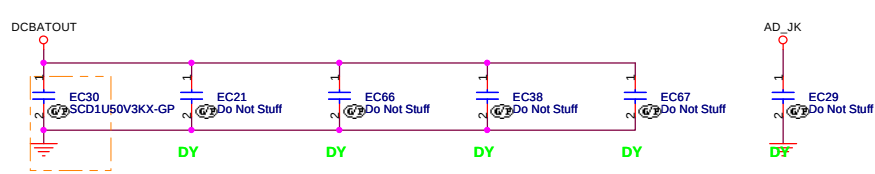
## AD/BATT CONN

**JE70-CP**

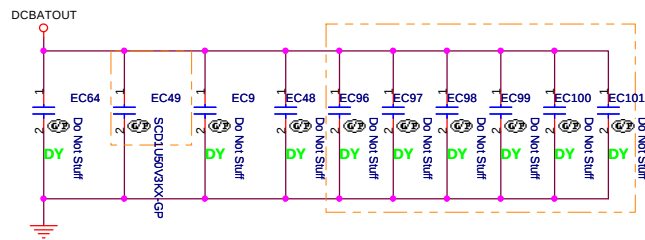
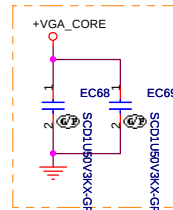
Date: Tuesday, February 02, 2010

Sheet 54 of 67

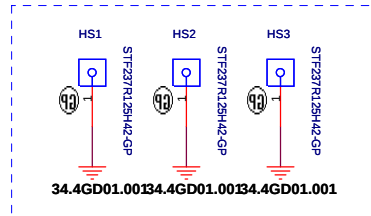
67



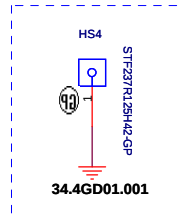
SB 1120



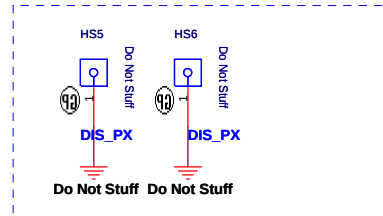
## CPU



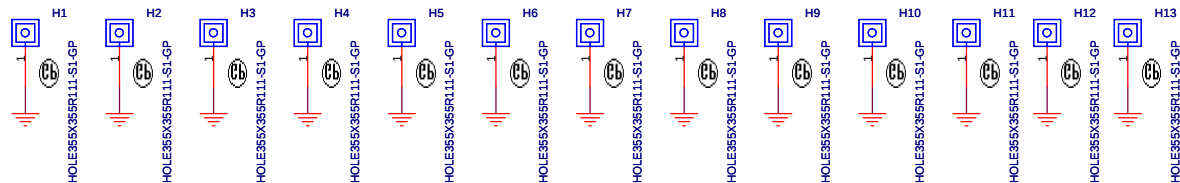
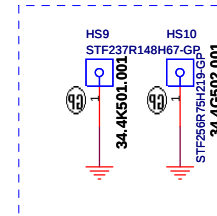
## PCH



## VGA



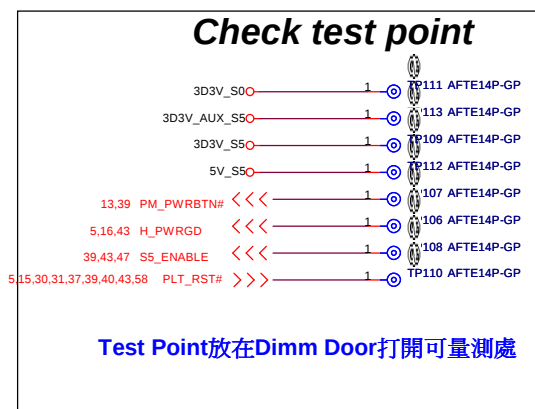
## MINICARD



Pre UMA

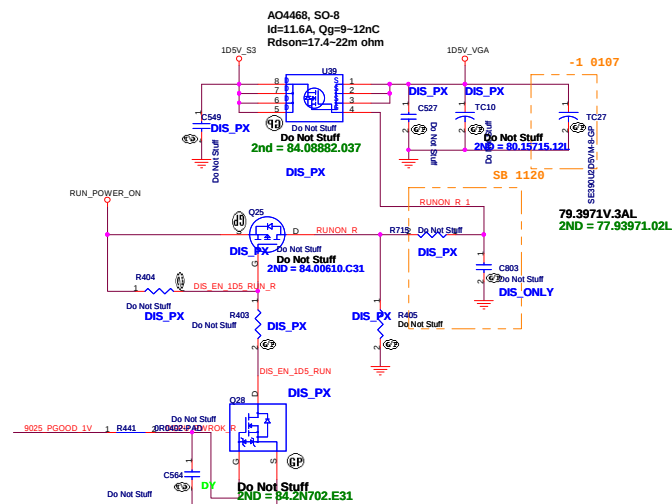
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|         |                            |       |                 |
|---------|----------------------------|-------|-----------------|
| Title   |                            |       | EMI/Spring/Boss |
| Size    | Document Number            | Rev   |                 |
| JE70-CP |                            |       | -1M             |
| Date:   | Tuesday, February 02, 2010 | Sheet | 55 of 67        |



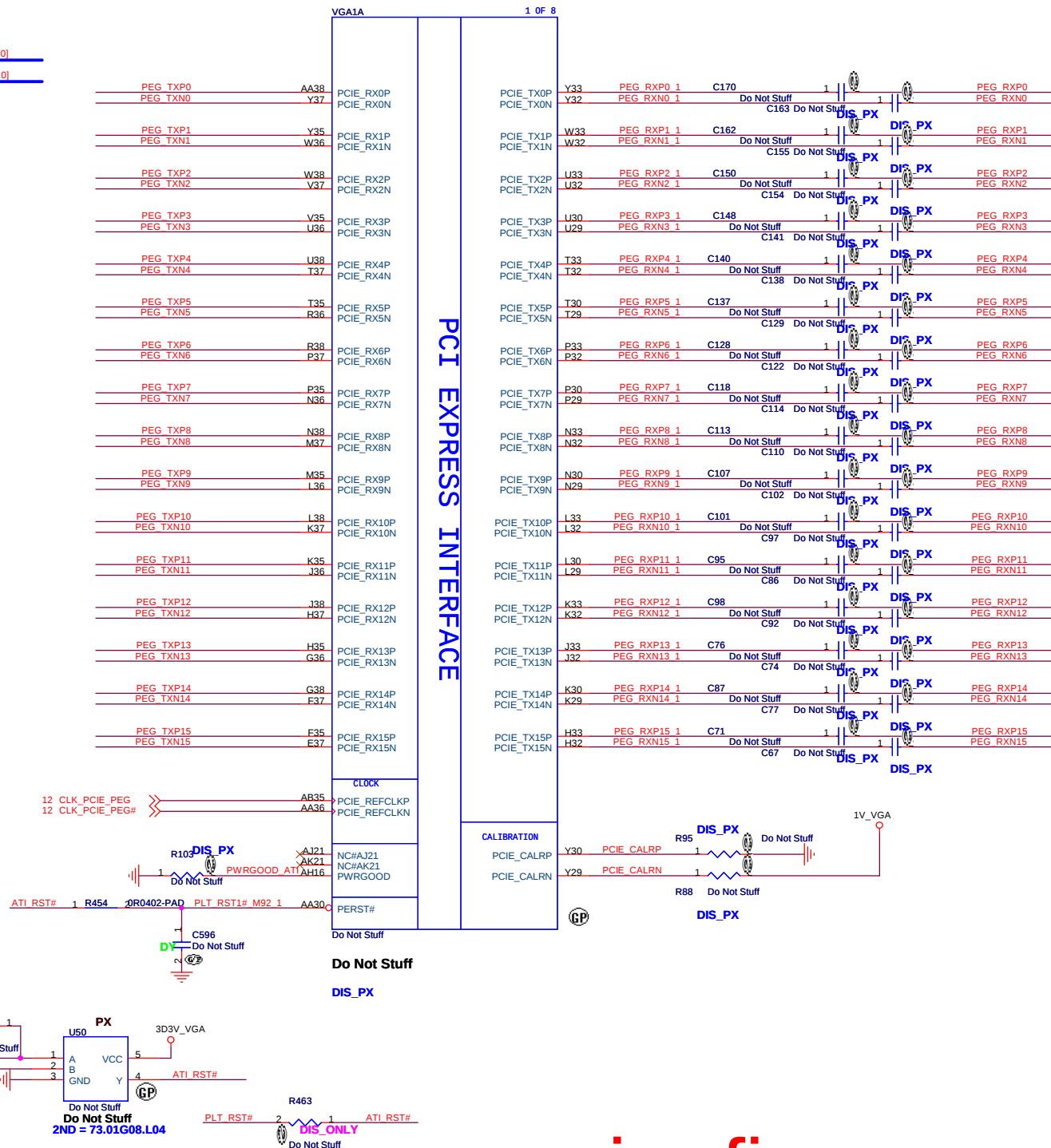
Pre UMA

|         |                            |                                                                            |                |
|---------|----------------------------|----------------------------------------------------------------------------|----------------|
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| AFTE TP |                            |                                                                            |                |
| Size    | Document Number            |                                                                            | Rev            |
|         | JE70-CP                    |                                                                            | -1M            |
| Date:   | Tuesday, February 02, 2010 |                                                                            | Sheet 56 of 67 |

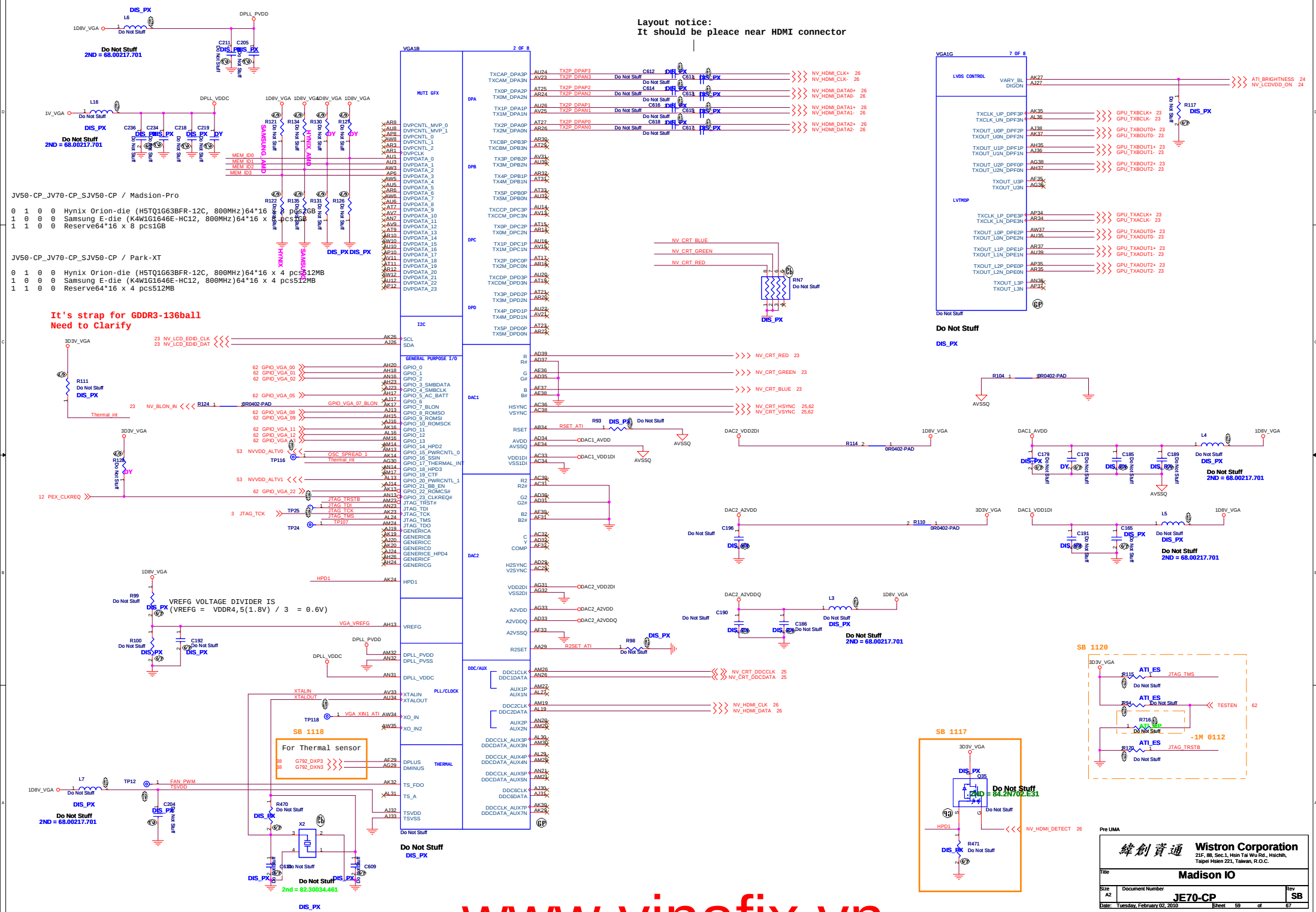
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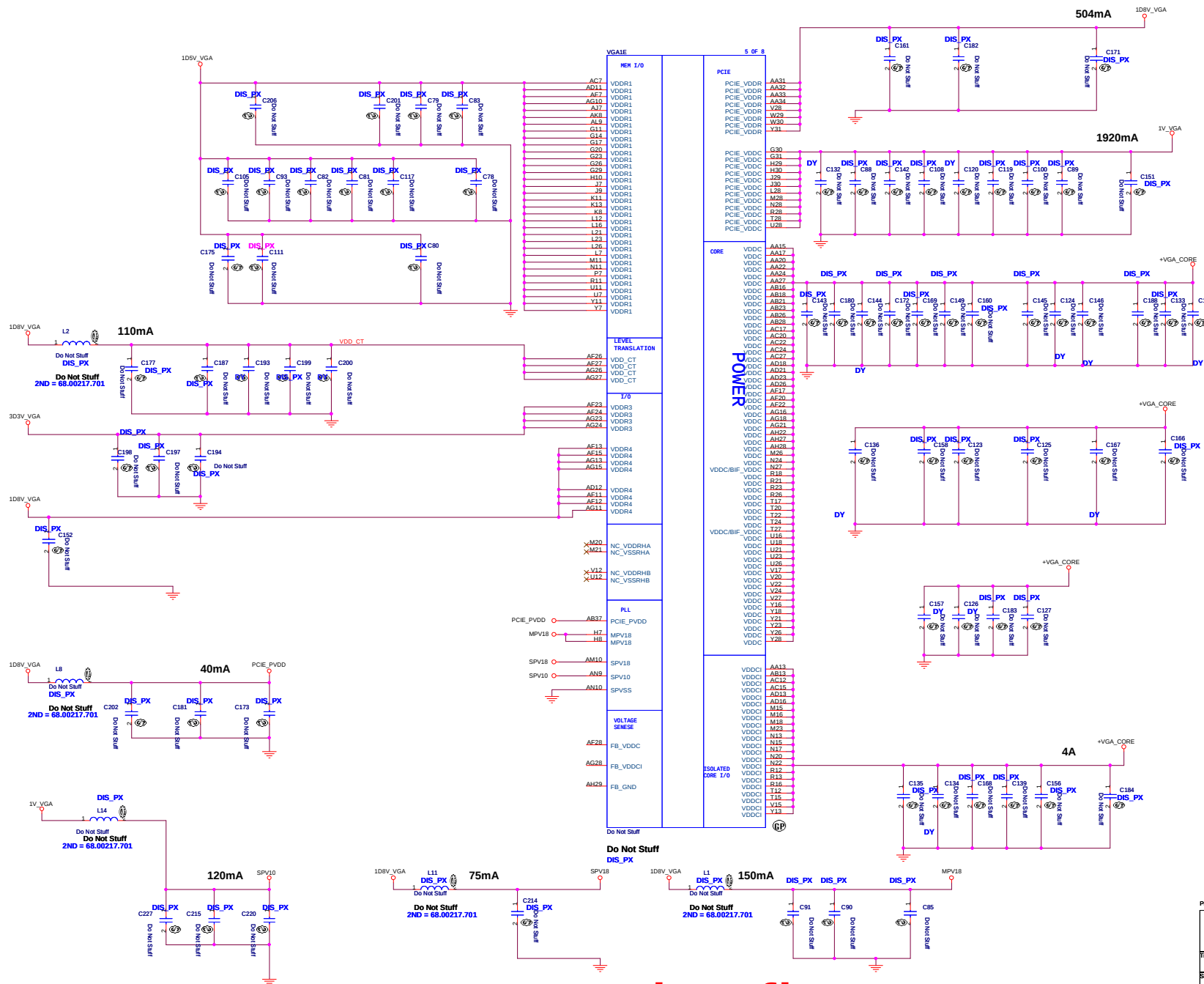
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4 PEG\_TXN[15..0] << PEG\_TXN[15..0]

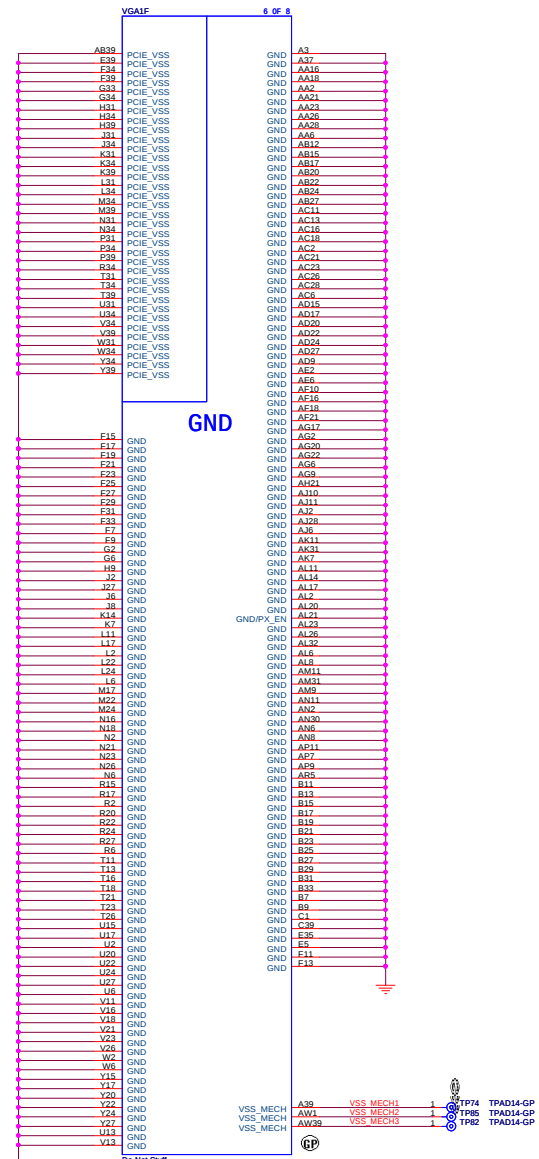
4 PEG\_RXP[15..0] << PEG\_RXP[15..0]  
4 PEG\_RXN[15..0] << PEG\_RXN[15..0]



Layout notice:  
It should be place near HDMI connector



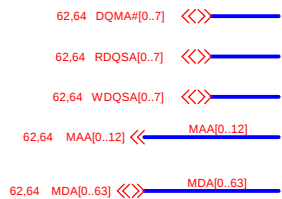
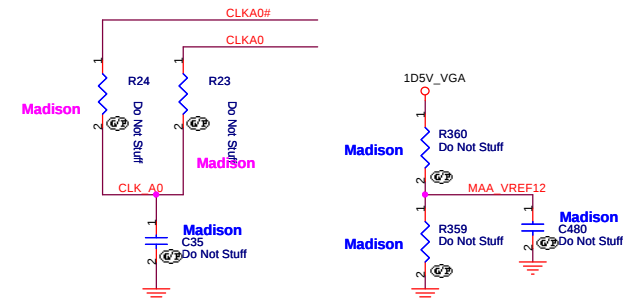




|              |                            |                                                                                                         |          |
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| Pre UIMA     |                            |                                                                                                         |          |
| 緯創資通         |                            | Wistron Corporation<br>21F, 88, Sec. 1, Hsien Tai Wu Rd., Hsichien,<br>Taipei Hsien 221, Taiwan, R.O.C. |          |
| File         |                            |                                                                                                         |          |
| DP POWER_GND |                            |                                                                                                         |          |
| Size<br>A2   | Document Number            | Rev                                                                                                     |          |
|              | JE70-CP                    | -1M                                                                                                     |          |
| Date:        | Tuesday, February 02, 2010 | Sheet                                                                                                   | 61 of 67 |



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|                                                                                                                                                                                                  |                 |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|
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| Title                                                                                                                                                                                            |                 |
| <b>VRAM(1/4)</b>                                                                                                                                                                                 |                 |
| Size<br>A3                                                                                                                                                                                       | Document Number |
| <b>JE70-CP</b>                                                                                                                                                                                   |                 |
| Date: Tuesday, February 02, 2010                                                                                                                                                                 | Sheet 63 of 67  |
| <b>-1M</b>                                                                                                                                                                                       |                 |

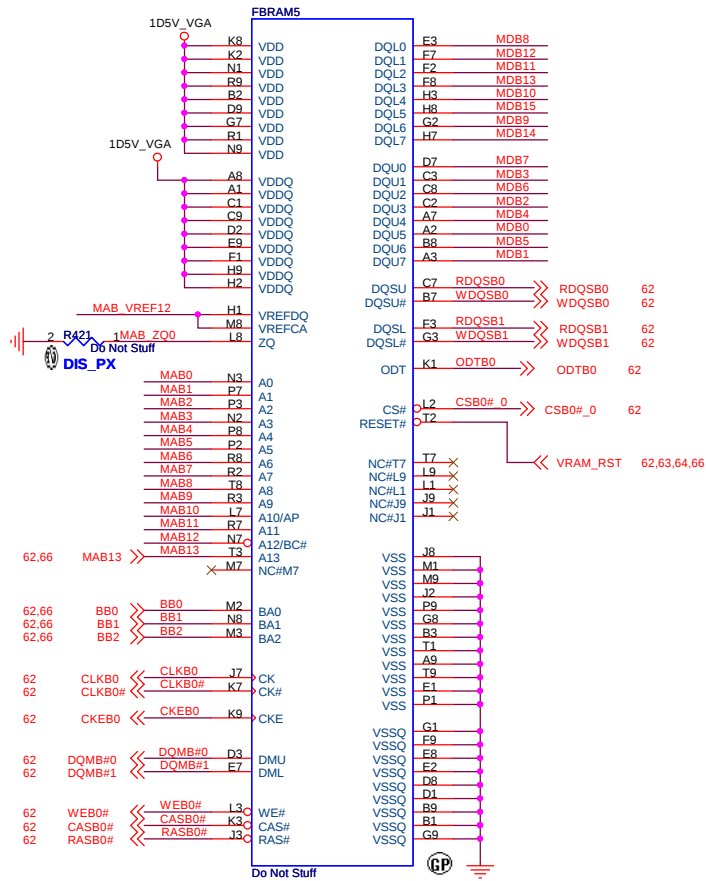
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The image contains two circuit diagrams for the Madison board. The top diagram shows the CLK\_A1 signal path, which is a differential pair of resistors (R356, R357) connected to a differential input (CLK\_A1#) and a differential output (CLK\_A1). The bottom diagram shows the 1D5V\_VGA signal path, which is a single-ended signal connected to a resistor (R26) and a differential input (MAA\_VREF34). Both diagrams include ground connections and labels for the components and signals.

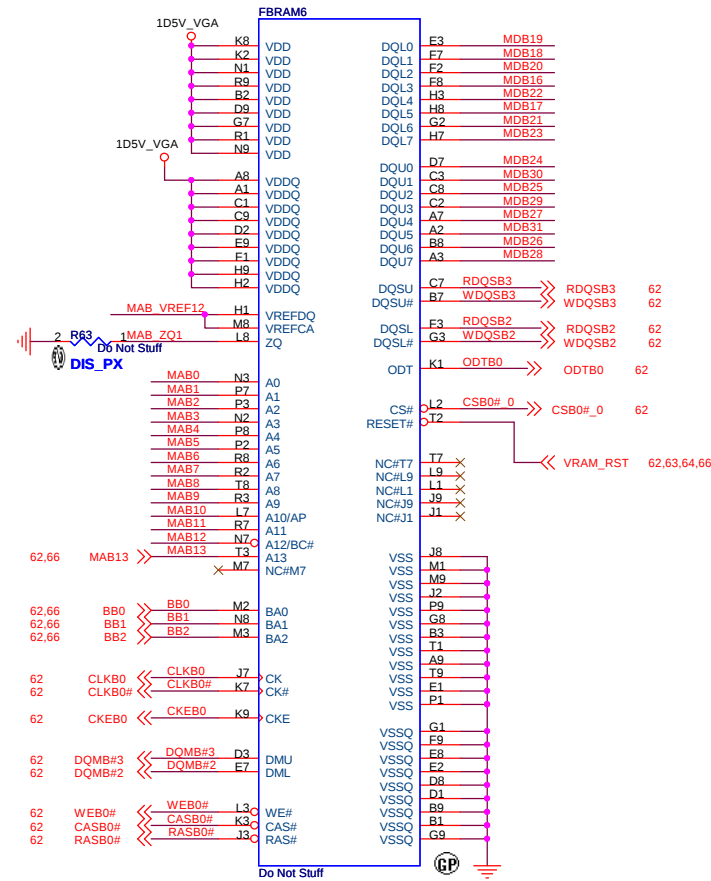
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| VRAM(2/4)  |                            |             |     |
| Size<br>A3 | Document Number            |             | Rev |
|            | JE70-CP                    |             | -1M |
| Date:      | Tuesday, February 02, 2010 | Sheet 64 of | 67  |

# DDR3



DIS\_PX

Do Not Stuff



DIS\_PX

Do Not Stuff

SAMSUNG: 72.41164.H0U

HYNIX: 72.51G63.C0U

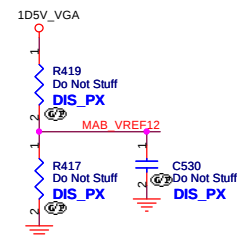
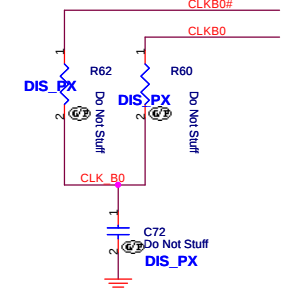
62,66 DQMB#[0..7] <<>

62,66 RDQSB#[0..7] <<>

62,66 WDQSB#[0..7] <<>

62,66 MAB[0..12] << MAB[0..12]

62,66 MDB[0..63] <<> MDB[0..63]



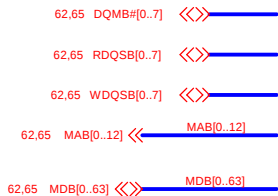
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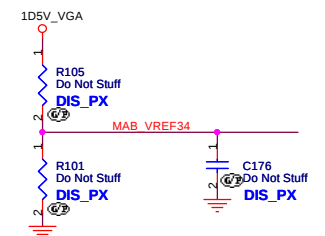
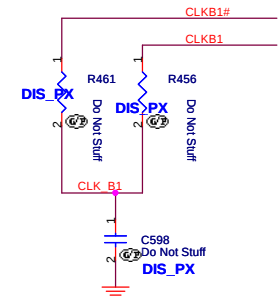
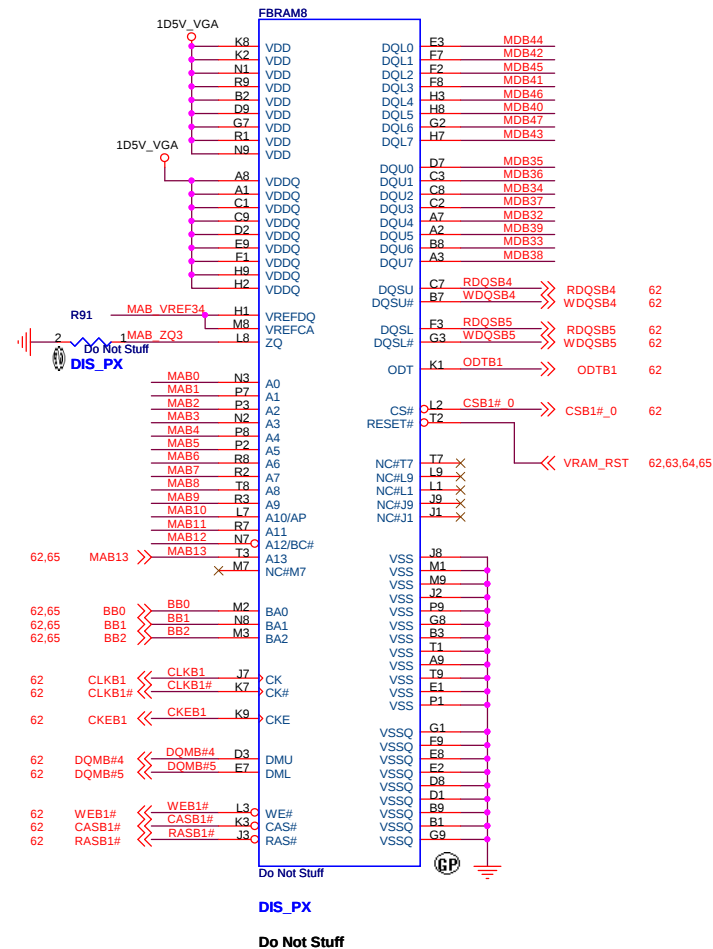
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|----------------------------------|-----------------|-----|
| VRAM(3/4)                        |                 |     |
| Size                             | Document Number | Rev |
| A3                               | JE70-CP         | -1M |
| Date: Tuesday, February 02, 2010 | Sheet 65 of 67  |     |

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| Title                 |                            |                                                                               |                |
| <b>Modify History</b> |                            |                                                                               |                |
| Size                  | Document Number            |                                                                               | Rev            |
|                       | <b>JE70-CP</b>             |                                                                               | <b>-1M</b>     |
| Date:                 | Tuesday, February 02, 2010 |                                                                               | Sheet 67 of 67 |